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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,947	03/31/2004	Seikoh Yoshida	2036-0104008Reg	4922

41646 7590 08/26/2005

FURUKAWA ELECTRIC NORTH AMERICA, INC.
1940 DUKE ST
SUITE 200
ALEXANDRIA, VA 22314

EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,947	YOSHIDA, SEIKOH	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 0104*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/31/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the application filed March 31, 2004.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

3. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moku et al. (Japanese Publication No. 2003-059948-Translation) in view of Applicant's Prior Art.

In regards to claim 1, Moku et al. ("Moku") discloses the following:

a) a substrate (1) (For Example: Figure 1);

b) a semiconductor layer structure including a buffer layer (2) structure, a channel layer (10) that are consecutively formed in this order on said substrate;

c) buffer layer structure includes at least one first buffer layer (9) comprising as a main component thereof a compound semiconductor expressed by the general formula of $Al_XIN_YGA_{1-X-Y}As_UP_VN_{1-U-V}$ (where $0\leq X\leq 1$, $0\leq Y\leq 1$, $X+Y\leq 1$, $0\leq U<1$, $0\leq V<1$, $U+V<1$); and at least one second buffer layer (8) comprising as a main component thereof a compound semiconductor expressed by the general formula of $Al_aIN_bGA_{1-a-b}As_cP_dN_{1-c-d}$ (where $0\leq A\leq 1$, $0\leq B\leq 1$, $A+B\leq 1$, $0\leq C<1$, $0\leq D<1$, $C+D<1$) and wherein said first buffer layer and said second buffer layer have different bandgap energies, and have two-dimensional electron gas density or densities therein not greater than $5x10^{12}cm^{-2}$ (Note: For Example: See Page 5 of 10 Paragraphs 16-18)(Note: Although Moku fails to specifically disclose that the first buffer layer and said second buffer layer have different bandgap energies, and that the two buffer layers have two-dimensional electron gas density or densities therein not greater than $5x10^{12}cm^{-2}$, the same material is utilized in Moku as in Applicant's invention therefore it would have the same characteristics).

In regards to claim 1, Moku fails to disclose the following:

a) a donor layer.

However, Applicant's Prior Art discloses a donor layer (15) (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Moku to include a donor layer as disclosed in Applicant's Prior Art because it aids in the formation of a lateral FET (For Example: See Column 2 Lines 14-23).

Additionally, since Moku and Applicant's Prior Art are both from the same field of endeavor, the purpose disclosed by Applicant's Prior Art would have been recognized in the pertinent art of Moku.

In regards to claims 2 and 7, Moku discloses the following:

a) the first buffer layer has a thickness of not less than .5nm and not greater than 20nm, and said second buffer layer has a thickness of not less than .5nm and not greater than 20nm (For Example: See Page 2 of 10 Paragraph 9)(Note: In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. See MPEP § 2144.05.).

In regards to claims 3 and 8, Moku discloses the following:

a) the second buffer layer has bandgap energy greater than a bandgap energy of said first buffer and has an Al composition not less than a thickness of not less than .5 and a thickness not less than 1 nm and nor greater than 10nm (For Example: See Page 2 of 10 Paragraph 9, Page 2 of 5 Paragraph 35, Page 8 of 10 Paragraph 34)(Note: In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. See MPEP § 2144.05.).

In regards to claim 6, Moku discloses the following:

a) buffer layer structure includes a plurality of said first buffer layers and a plurality of second buffer layers which are alternately laid on one another (For Example: See Figure 1).

Allowable Subject Matter

6. Claims 4, 5, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance:

In regards to claims 4 and 9, the prior art fails to disclose the following: a) the first and second buffer layers comprise one of Mg, Be, Zn and C in an amount of not less than $1x10^{16}$ cm^{-3} and not greater than $1x10^{16}$ cm^{-3}.

In regards to claims 5 and 10, the prior art fails to disclose the following: a) an operating current of not less than 1 ampere or an operating voltage of not less than 100 volts.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) *Photoluminescence Characterization of P-Type GaN:Mg* by Corlatan et al.; b) Tsuchiya et al. (Japanese Publication No. 2002-050758) discloses a compound semiconductor epitaxial wafer and transistor; c) Furukawa (Japanese Publication No. 2001-274376) discloses a low resistant gallium nitride group buffer layer; d) Maeda et al. (Japanese Publication No. 2001-326232) discloses a semiconductor device; e) *Growth of High-Performance GaN Modulation Doped Field Effect Transistors by Ammonia Molecular Beam Epitaxy* by Tang et al.; and f) Reproducibility of Growing AlGaN/GaN High-Electron-Mobility-Transistor Heterostructures by Molecular-Beam Epitaxy by Tang et al.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956

ML

August 12, 2005

2822

3/31/04

Substitute for form 1449B/PTO				Complete If Known	
INFORMATION DISCLOSURE				Application Number	New Application
				Filing Date	Filed Herewith
STATEMENT BY APPLICANT				First Named Inventor	Seikoh YOSHIDA
				Art Unit	
(Use as many sheets as necessary)				Examiner Name	
Sheet	1	of	1	Agent Docket Number	2036-0104008Reg

U.S. Patent Documents

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, where Relevant Passages or Relevant Figures Appear
		US-			
		US-			
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Foreign Patent Documents

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2](if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, where Relevant Passages or Relevant Figures Appear	T[6]
MC		2003-059948	02-28-2003	Tetsuji MOKU	—	

Examiner Signature		Date Considered	8/11/04

Notice of References Cited	Application/Control No. 10/812,947	Applicant(s)/Patent Under Reexamination YOSHIDA, SEIKOH	
	Examiner Monica Lewis	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	2003-059948-English Trans	02-2003	Japan	Moku et al.	H01L 21/338
	O					
	P	2002-198483	10-2001	Japan	Furukawa	H01L 029/778
	Q	2002-50758	02-2002	Japan	Tsuchiya et al.	H01L 29/778
	R	2001-326232	11-2001	Japan	Maeda et al.	H01L 21/338
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Tang et al., Reproducibility of growing AlGaN/GaN high-electron-mobility-transistor heterostructures by molecular-beam epitaxy, Solid-State Electronics, 2000, pages 2177-2182.
	V	Tang et al., Growth of high-performance GaN modulation-doped field-effect transistors by ammonia-molecular-beam epitaxy, Journal of Vacuum Science & Technology, 2000, pages 652-655.
	W	Corlatan et al., Photoluminescence characterization of p-type GaN:Mg, Materials Research Society, 1998, pages 673-678.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

L143 ANSWER 11 OF 26 CAPLUS **COPYRIGHT ACS on STN**

AN 2002:119796 CAPLUS
DN 136:176503
TI **Compound semiconductor** epitaxial wafers for heterojunction transistors
IN Tsuchiya, Tadayoshi; Kihara, Norio
PA Hitachi Cable, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2002050758	A2	20020215	JP 2000-240379	20000803
PRAI JP 2000-240379		20000803		

AB **Buffer layers** contg. at least AlGaN among GaN, AlGaN and AlN are formed on sapphire **substrates**, and heterojunctions comprising GaN **channel layers** and AlGaN carrier supplying **layers** are formed on the **buffer layers**, where the **buffer layers** have no smaller linear expansion coeff. than the carrier supplying **layers**. Extension deformation in the carrier supplying **layers** is moderated. 2-Dimensional hole gas can be generated while suppressing electron formation at the heterojunction interfaces, and hole-carrier p-type FETs can be realized.

IT **25617-97-4**, Gallium **nitride** (GaN) **117656-36-7**, Aluminum gallium nitride (Al0.3Ga0.7N)
RL: DEV (Device component use); USES (Uses)
(**buffer layer**; **compd. semiconductor** epitaxial wafers for heterojunction transistors)
RN 25617-97-4 CAPLUS
CN Gallium nitride (GaN) (6CI, 8CI, 9CI) (CA INDEX NAME)

RN 117656-36-7 CAPLUS
CN Aluminum gallium nitride (Al0.3Ga0.7N) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	1	17778-88-0
Ga	0.7	7440-55-3
Al	0.3	7429-90-5

IT **125297-45-2**, Aluminum gallium nitride (Al0.2Ga0.8N)
RL: DEV (Device component use); USES (Uses)
(carrier supplying layer; **compd. semiconductor** epitaxial wafers for heterojunction transistors)
RN 125297-45-2 CAPLUS
CN Aluminum gallium nitride (Al0.2Ga0.8N) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号
特開2002－50758
（P2002－50758A）
(43)公開日　平成14年２月15日(2002.2.15)

(51)Int.Cl.⁷		識別記号	FI		テーマコード（参考）
H01L	29/778		C30B	29/40	502H　4G077
	21/338		H01L	21/205	5F045
	29/812			29/80	H　5F102
C30B	29/40	502			
H01L	21/205				

審査請求　未請求　請求項の数３　ＯＬ　（全４頁）

(21)出願番号　特願2000－240379(P2000－240379)

(22)出願日　平成12年８月３日(2000.8.3)

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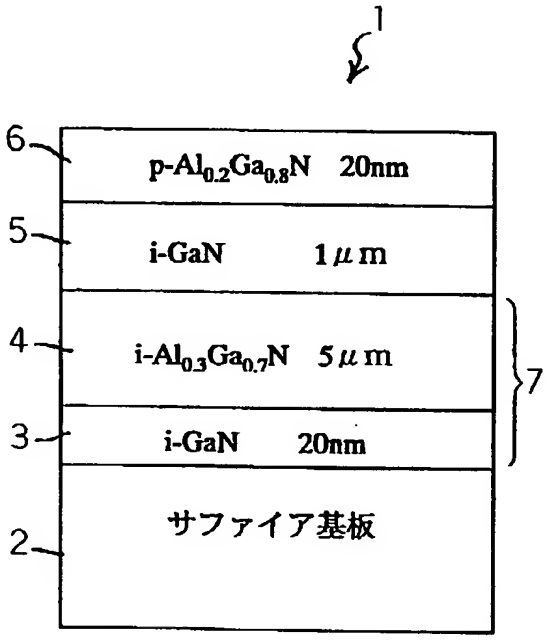
最終頁に続く

(54)【発明の名称】　化合物半導体エピタキシャルウェハ及びそれを用いたトランジスタ

(57)【要約】
【課題】　正孔をキャリアとする化合物半導体エピタキシャルウェハ及びそれを用いたトランジスタを提供する。
【解決手段】　チャネル層５の下部に、キャリア供給層６と線膨張係数が等しいか大きいバッファ層７を十分な厚さで挿入することにより、キャリア供給層６に生じる引っ張り歪を緩和し、ヘテロ界面への電子の誘起を押さえて２次元正孔ガスを発生させることができ、この結果、正孔をキャリアとするｐ型ＦＥＴを実現することができる。



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【特許請求の範囲】

【請求項1】　サファイア基板上に、GaN、AlGaN及びAlNのうち少なくともAlGaNを有するバッファ層を形成し、該バッファ層の上にGaN及びp型AlGaNのヘテロ接合を形成し、上記バッファ層のAlGaN層の膜厚をエピタキシャルウェハ全体におけるGaN層の膜厚より厚くしたことを特徴とする化合物半導体エピタキシャルウェハ。

【請求項2】　請求項1において、上記バッファ層のAlGaNのAlNの組成比がp型AlGaNのAlN組成比より高い化合物半導体エピタキシャルウェハ。

【請求項3】　請求項1または2に記載のエピタキシャルウェハを用いた化合物半導体エピタキシャルウェハを用いたトランジスタ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、化合物半導体エピタキシャルウェハ及びそれを用いたトランジスタに関する。

【0002】

【従来の技術】窒化ガリウム系の電界効果トランジスタ（以下「FET」という。）としては、従来、n型GaNをチャンネル層とするFET及びn型AlGaN／GaN選択ドープ構造を有するFETの研究開発が進められている。

【0003】

【発明が解決しようとする課題】ところで、上述した従来技術のFETは全てデバイス動作に関わる主たるキャリアが電子のn型FETである。ここで、正孔をキャリアとするp型FETがあれば、C－MOSトランジスタのように相補型のFETが実現でき、負電源が不要になる。

【0004】しかしながら正孔をキャリアとするFETは実用化が困難である。特に、p型AlGaN／GaN選択ドープ構造では、ピエゾ効果のために界面に電子が誘起され、所望の正孔を発生させることができないという問題があった。

【0005】そこで、本発明の目的は、上記課題を解決し、正孔をキャリアとする化合物半導体エピタキシャルウェハ及びそれを用いたトランジスタを提供することにある。

【0006】

【課題を解決するための手段】上記目的を達成するために本発明の化合物半導体エピタキシャルウェハは、サファイア基板上に、GaN、AlGaN及びAlNのうち少なくともAlGaNを有するバッファ層を形成し、バッファ層の上にGaN及びp型AlGaNのヘテロ接合を形成し、バッファ層のAlGaN層の膜厚をエピタキシャルウェハ全体におけるGaN層の膜厚より厚くしたものである。

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【0007】上記構成に加え本発明の化合物半導体エピタキシャルウェハは、バッファ層のAlGaNのAlNの組成比がp型AlGaNのAlN組成比より高いのが好ましい。

【0008】本発明のトランジスタは上記構成のエピタキシャルウェハを用いたものである。

【0009】本発明によれば、p型AlGaN／GaN選択ドープ構造で、界面に電子が誘起される原因は、キャリア供給層であるAlGaNがチャネル層であるGaNより線膨張係数が大きいため、AlGaNキャリア供給層に成膜後の冷却中に弾性応力によって生じる引っ張り歪である。AlGaNキャリア供給層のピエゾ効果が大きいため、この引っ張り歪に応じて界面にキャリアが誘起される。GaN系の材料のエピタキシャル成長用の基板には、通常サファイアもしくはSiCの単結晶が用いられる。この基板の上にGaNをc軸配向して成長させる場合、Ga面が上になるように成長（Ga面成長）させる方法が安定であることが知られている。このGa面成長はピエゾ分極の方向が必ず界面に電子を誘起する方向となり、正孔を界面に形成する阻害要因となる。界面に正孔を誘起するためには、Ga面とは反対のN面が上になる成長（N面成長）が必要となるが、このN面成長は不安定な成長となり、良い結晶が得られない。

【0010】本発明ではチャネル層となるGaN層の下部に、AlGaNキャリア供給層と線膨張係数が等しいか大きいバッファ層を十分な厚さで挿入することにより、AlGaNキャリア供給層に生じる引っ張り歪を緩和し、ヘテロ界面への電子の誘起を押さえて2次元正孔ガスを発生させることができ、この結果、正孔をキャリアとするp型FETを実現することができる。

【0011】

【発明の実施の形態】以下、本発明の実施の形態を添付図面に基づいて詳述する。

【0012】図1は本発明の化合物半導体エピタキシャルウェハの一実施の形態を示す構造図である。

【0013】同図に示すエピタキシャルウェハ1は、サファイア基板2上に、厚さ20nmのi－GaN層3、厚さ5μmのi－$Al_{0.3}Ga_{0.7}N$層4、厚さ1μmのチャネル層としてのi－GaN層5及び厚さ20nmのキャリア供給層としてのp－$Al_{0.2}Ga_{0.8}N$層6を順次形成したものである。

【0014】i－$Al_{0.3}Ga_{0.7}N$層4及びi－GaN層5でバッファ層7を形成し、p－$Al_{0.2}Ga_{0.8}N$層4及びi－GaN層5でヘテロ接合を形成している。

【0015】このエピタキシャルウェハ1のエピタキシャル成長には有機金属気相成長法を用いた。ガリウム原料にはTMG（トリメチルガリウム）を用い、アルミニウム原料にはTMA（トリメチルアルミニウム）を用い、窒素原料にはアンモニアガスを用い、p型ドーパン

トとしては、ビスシクロペンタマグネシウムを用いた。シリコン原料にはモノシランを用いた。エピタキシャル成長はフェイスアップの高周波誘導加熱横型減圧炉（図示せず。）を用いて炉内圧力17955Pa（135Torr）で行った。基板2にはA面及びC面のサファイア単結晶基板を用いた。エピタキシャル成長時の基板温度は1050℃である。

【0016】このようにして成長させたエピタキシャルウェハ1のC－V測定で求めたキャリア濃度プロファイルを図2に示す。

＊【0017】図2は図1に示したエピタキシャルウェハのキャリア濃度と深さとの関係を示す図であり、横軸が深さ軸を示し、縦軸がキャリア濃度軸を示す。

【0018】同図よりピークは界面に2次元正孔ガスが生じていることを示しており、従来の問題点は解決できることが分った。このピークからシート正孔濃度を求め、バッファ層7に用いられているAlGaNの組成、膜厚との関係を示したのが表1である。

【0019】

＊10　【表1】

	AlN組成比	膜厚(nm)	シート濃度(cm-2)
標準	0.3	5000	1.20E+13
組成比依存性	0	5000	測定不可
	0.1		5.00E+11
	0.2		1.00E+13
	0.5		1.25E+13
	1		1.30E+13
膜厚依存性	0.3	3000	1.20E+13
		2000	1.20E+13
		1000	1.00E+13
		50	測定不可

【0020】同表より、AlGaNのAlN組成比を供給層の組成比より下げたり、あるいは膜厚をGaNの総膜厚より薄くした場合に、2次元正孔ガスの濃度が低下する傾向があることが分る。これは、前述のようにバッファ層7のAlGaNバッファ層4の効果が薄れてGaN層3の影響が相対的に高まったためと見られる。

【0021】図3は図1に示したエピタキシャルウェハを用いたトランジスタの構造図である。なお、数値については限定されるものではない。

【0022】図3に示すトランジスタ10は、サファイア基板2上に、厚さ20nmのi－GaN層3、厚さ5μmのi－$Al_{0.3}Ga_{0.7}N$層4、厚さ1μmのチャネル層としてのi－GaN層5及び厚さ20nmのキャリア供給層としてのp－$Al_{0.2}Ga_{0.8}N$層6を順次形成し、このp－$Al_{0.2}Ga_{0.8}N$層6の上にソース電極11、ゲート電極（ゲート長さLg＝1μm）12及びドレイン電極13を形成したものである。

【0023】図4は図3に示したトランジスタの静特性を示す図であり、横軸がドレイン電圧Vd軸を示し、縦軸がドレイン電流Id軸を示す。

【0024】同図より、p型FETが通常のn型FETと同様の静特性を有することが分る。

【0025】ここで、バッファ層7としては、（GaN、AlGaN）、（AlN、AlGaN）、（AlN、GaN、AlGaN）、（GaN、AlGaN、GaN、AlGaN）、（AlN、AlGaN、GaN、AlGaN）、（GaN、$Al_{0.3}Ga_{0.1}N$、$Al_{0.1}Ga_{0.9}N$、$Al_{0.3}Ga_{0.7}N$）の組み合わせが挙げられる。但し、（）内の左側が基板側、右側が電極※側になる。

【0026】このように構成したことで、チャネル層5の下部に、キャリア供給層6と線膨張係数が等しいか大きなAlGaNバッファ層4を挿入する場合、チャネル層5とAlGaNバッファ層4との間の格子定数の違いに起因する臨界膜厚が存在する。この臨界膜厚を超える厚さで挿入すると、結晶性欠陥が生じてデバイス特性の劣化を招くおそれがある。この劣化を防止するためには、サファイア基板2上にもしGaNバッファ層3を成長させたい場合でも、このGaNバッファ層3を500℃付近で成長させる、いわゆる低温成長バッファのみとし、その他のバッファ層はAlGaN層とすることによって、積層構造全体としての線膨張係数をキャリア供給層6に近付け、それによってAlGaNバッファ層4の弾性歪を低減する方法が有効である。この場合はGaNバッファ層3が圧縮応力を受けるが、本発明ではGaNバッファ層3として必要な厚さが薄いため、問題が生じない。

【0027】以上において本発明の化合物半導体エピタキシャルウェハを用いたトランジスタによるp型FETを、n型FETと組み合わせることで相補型のトランジスタを構成することができ、負電源が不要になり、回路構成が簡単になり、小形化、低コスト化が図れる。

【0028】

【発明の効果】以上要するに本発明によれば、次のような優れた効果を発揮する。

【0029】正孔をキャリアとする化合物半導体エピタキシャルウェハ及びそれを用いたトランジスタの提供を実現することができる。

【図面の簡単な説明】

【図1】本発明の化合物半導体エピタキシャルウェハの一実施の形態を示す構造図である。

【図2】図1に示したエピタキシャルウェハのキャリア濃度と深さとの関係を示す図である。

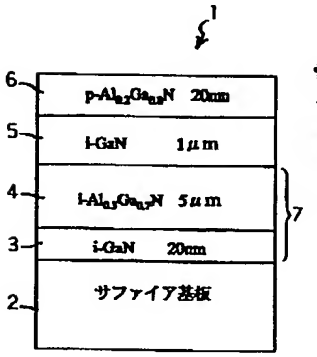
【図3】図1に示したエピタキシャルウェハを用いたトランジスタの構造図である。

【図4】図3に示したトランジスタの静特性を示す図である。

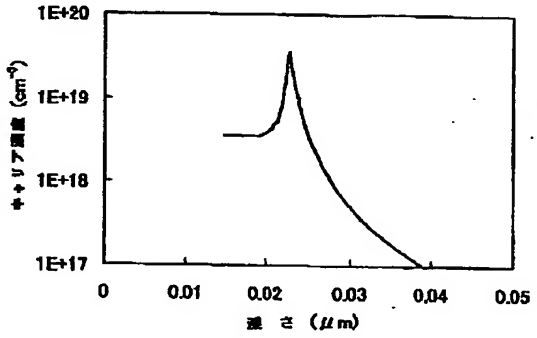
【符号の説明】

2　サファイア基板
3　GaN層（GaNバッファ層）
4　AlGaN層（AlGaNバッファ層）
5　GaN層（チャネル層）
6　AlGaN層（キャリア供給層）
7　バッファ層

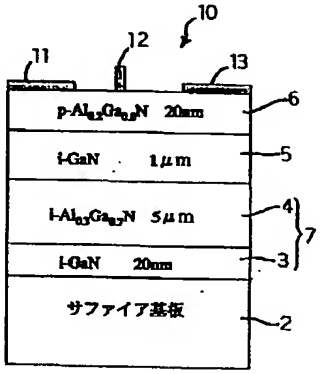
【図1】



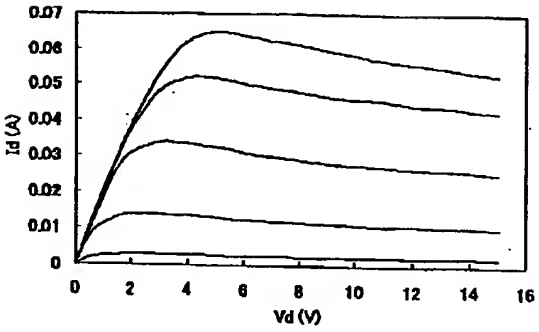
【図2】



【図3】



【図4】



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L143 ANSWER 13 OF 26 CAPLUS **COPYRIGHT ACS on STN**

AN 2001:847814 CAPLUS
DN 135:379674
TI Semiconductor device.
IN Maeda, Yukihiko; Kobayashi, Naoki
PA Nippon Telegraph and Telephone Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2001326232	A2	20011122	JP 2000-139760	20000512
PRAI JP 2000-139760		20000512		

AB A semiconductor device having high-temp. and high-withstand-**voltage** operation properties comprises a **semiconductor** substrate having a **nitride semiconductor buffer** layer and an AlxGa1-xN **channel layer** (0 < x < 1) on the **buffer** layer. Specifically, the substrate may comprise a SiC, sapphire, or GaN substrate. Addnl., the device may have a GaN layer between the **buffer** and **channel layers**. The device is useful as a FET.

IT **25617-97-4**, Gallium nitride (GaN) **106097-44-3**, Aluminum gallium nitride ((Al,Ga)N) **120994-23-2**, Gallium indium nitride
RL: DEV (Device component use); USES (Uses)
(AlxGa1-xN **channel layer** of semiconductor device)

RN 25617-97-4 CAPLUS
CN Gallium nitride (GaN) (6CI, 8CI, 9CI) (CA INDEX NAME)

RN 106097-44-3 CAPLUS
CN Aluminum gallium nitride ((Al,Ga)N) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	1	17778-88-0
Ga	0 - 1	7440-55-3
Al	0 - 1	7429-90-5

RN 120994-23-2 CAPLUS
CN Gallium indium nitride ((Ga,In)N) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
N	1	17778-88-0
In	0 - 1	7440-74-6
Ga	0 - 1	7440-55-3

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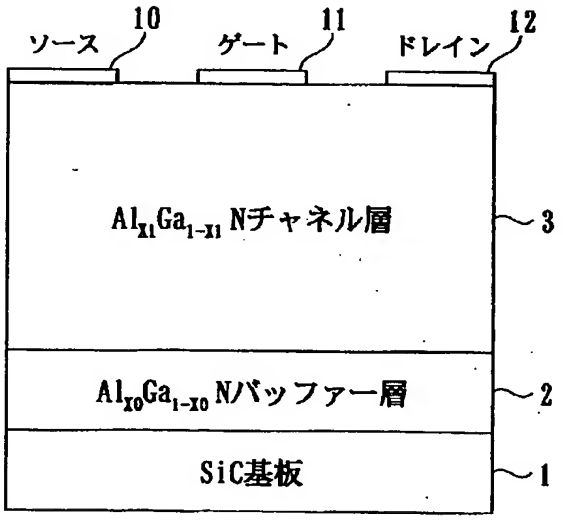
GJ02 GJ10 GK04 GK08 GL04
GM04 GQ01

(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　従来のＧａＮ系デバイスよりも高温動作特性・高耐圧動作特性を向上させる。
【解決手段】　半導体基板と、この半導体基板上に形成された窒化物半導体のバッファ層と、このバッファ層よりも上層に形成された窒化物半導体のチャネル層とを備える。前記チャネル層は、$Al_xGa_{1-x}N$層（０＜Ｘ＜１）によって形成されている。



$0<X0\leqq 1$，$0<X1<1$

1

【特許請求の範囲】

【請求項1】　半導体基板と、この半導体基板上に形成された窒化物半導体のバッファ層と、このバッファ層よりも上層に形成された窒化物半導体のチャネル層とを備え、

前記チャネル層は、$Al_xGa_{1-x}N$（0<X<1）によって形成されていることを特徴とする半導体装置。

【請求項2】　請求項1に記載の半導体装置において、前記チャネル層上に形成されたソース電極、ゲート電極およびドレイン電極を備え、電界効果トランジスタを構成していることを特徴とする半導体装置。

【請求項3】　請求項1に記載の半導体装置において、前記チャネル層上に形成された窒化物半導体の障壁層と、

この障壁層上に形成されたソース電極、ゲート電極およびドレイン電極とを備え、ヘテロ構造電界効果トランジスタを構成していることを特徴とする半導体装置。

【請求項4】　請求項2または請求項3に記載の半導体装置において、

前記バッファ層と前記チャネル層との間に形成されたGaN層を備えたことを特徴とする半導体装置。

【請求項5】　半導体基板と、この半導体基板上に形成された窒化物半導体のバッファ層と、このバッファ層よりも上層に形成された窒化物半導体のチャネル層と、このチャネル層直下に形成された$Al_{x1}Ga_{1-x1}N$（0<X1<1）の第1の障壁層と、前記チャネル層直上に形成された$Al_{x2}Ga_{1-x2}N$（0<X2<1）の第2の障壁層と、この第2の障壁層上に形成されたソース電極、ゲート電極およびドレイン電極とを備え、

前記第1の障壁層のAl組成X1には、この第1の障壁層直下の層構造とAl組成不連続を起こさないように、深さ方向に減少する傾斜が施されていることを特徴とする半導体装置。

【請求項6】　請求項5において、

前記チャネル層は、GaN、$In_YGa_{1-Y}N$（0<Y≦1）、または$Al_ZGa_{1-Z}N$（0<Z≦1，Z<X1，Z<X2）の何れかで形成されていることを特徴とする半導体装置。

【請求項7】　請求項1または請求項5において、

前記半導体基板は、SiC基板、サファイア基板またはGaN基板であることを特徴とする半導体装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、半導体装置に関し、特に窒化物半導体を用いた半導体装置に関するものである。

【0002】

【従来の技術】従来、窒化物半導体を用いた電界効果トランジスタ（Field Effect Transistor:FET）またはヘテロ構造電界効果トランジスタ（Heterostructure Field Effect Transistor:HFET）においては、電子が走行するチャネル層にGaNや$In_xGa_{1-x}N$（0<X<1）が用いられている（特願平10-56529号、特願平10-69176号参照）。これらの材料を用いたデバイス（GaN系デバイス）は、従来のGaAs系のFETまたはHFETよりも高温・高耐圧動作が可能であることが上記特許出願の明細書に開示されている。

2

【0003】

【発明が解決しようとする課題】しかしながら、さらに高温・高耐圧動作を向上させるためには、半導体材料の結晶結合力が大きくなるようにチャネル材料を改良する必要がある。また、窒化物半導体を用いたヘテロ構造電界効果トランジスタ（HFET）においては、ヘテロ界面に特有の正または負の分極電荷が発生する。HFETがチャネル電子の形成されるヘテロ界面以外にもヘテロ界面を有し、このヘテロ界面が正の分極電荷を誘起する場合には、このヘテロ界面に電子が引きつけられ、チャネル電子層以外にも電子層が形成される。このような非チャネル電子の存在は、HFETの低周波動作に影響を与えないものの、HFETの高周波特性を劣化させる。電子が走行するチャネル層直下の障壁として$Al_xGa_{1-x}N$層（0<X<1）が設けられている場合に上述のような状況が起こり得、HFETを高周波デバイスとして用いる場合には、非チャネル電子を消滅させることにより、高周波特性を向上させる必要がある。本発明は、このような課題を解決するためのものであり、従来のGaN系デバイスよりも高温動作特性・高耐圧動作特性を向上させた半導体装置（FETおよびHFET）を提供することを目的とする。また、従来よりも高周波特性の優れた半導体装置（HFET）を提供することをその他の目的とする。

【0004】

【課題を解決するための手段】このような目的を達成するために、本発明に係る半導体装置は、半導体基板と、この半導体基板上に形成された窒化物半導体のバッファ層と、このバッファ層よりも上層に形成された窒化物半導体のチャネル層とを備え、前記チャネル層は、$Al_xGa_{1-x}N$層（0<X<1）によって形成されている。このような構成により本発明は、従来のGaNよりもバンドギャップの広い$Al_xGa_{1-x}N$を用いることにより、チャネル層における結晶結合力が大きくなり、高温動作特性・高耐圧動作特性を特に向上させることができる。これは窒化物半導体を用いたFETまたはHFETにおける高温・高耐圧動作は、半導体材料の大きな結合力によりもたらされ、一般的に結晶結合力とバンドギャップとの間には正の相関があり、バンドギャップの大きな半導体ほど大きな結晶結合力を持つことから、高温動作特性・高耐圧動作特性を向上させることができることによる。

【0005】また、本発明はその他の態様として以下に

示す構成を含むものである。すなわち、前記チャネル層上に形成されたソース電極、ゲート電極およびドレイン電極を備え、電界効果トランジスタを構成している。このように構成することにより本発明は、従来よりも高温動作特性・高耐圧動作特性を特に向上させた電界効果トランジスタを実現できる。また、前記チャネル層上に形成された窒化物半導体の障壁層と、この障壁層上に形成されたソース電極、ゲート電極およびドレイン電極とを備え、ヘテロ構造電界効果トランジスタを構成している。このように構成することにより本発明は、従来よりも高温動作特性・高耐圧動作特性を特に向上させたヘテロ構造電界効果トランジスタを実現できる。また、前記バッファ層の上に形成されたGaN層を備える。このように構成することにより本発明は、このGaN層上に形成される層（チャネル層等）の結晶性を向上させることができる。

【0006】さらに、半導体基板と、この半導体基板上に形成された窒化物半導体のバッファ層と、このバッファ層よりも上層に形成された窒化物半導体のチャネル層と、このチャネル層直下に形成された$Al_{x1}Ga_{1-x1}N$（$0<X1<1$）の第1の障壁層と、前記チャネル層直上に形成された$Al_{x2}Ga_{1-x2}N$（$0<X2<1$）の第2の障壁層と、この第2の障壁層上に形成されたソース電極、ゲート電極およびドレイン電極とを備え、前記第1の障壁層のA1組成X1には、この第1の障壁層直下の層構造とA1組成不連続を起こさないように、深さ方＊向に減少する傾斜が施されている。このように構成することにより本発明は、チャネル層の直下に設けられた$Al_xGa_{1-x}N$（$0<X<1$）に副次的電子層が発生することを防止することができ、HFETの高周波特性を特に向上できる。なお、前記チャネル層は、GaN、$In_yGa_{1-y}N$（$0<Y\leqq1$）、または$Al_zGa_{1-z}N$（$0<Z\leqq1$，$Z<X1$，$Z<X2$）の何れかで形成されていてもよい。また、前記半導体基板は、SiC基板、サファイア基板またはGaN基板であってもよい。

【0007】

【発明の実施の形態】次に、本発明の一つの実施の形態（層構造）について説明する。本発明においては、従来のGaN系材料よりもバンドギャップの大きな材料でチャネル層を形成することにより、高温動作特性・高耐圧動作特性を向上させる。例えばこのような条件を満たす材料として、$Al_xGa_{1-x}N$（$0<X<1$）を用いるとよい。

【0008】ここで、$Al_xGa_{1-x}N$（$0<X<1$）のバンドギャップについて説明する。GaNのバンドギャップEg（GaN）の大きさが3．4、AlGaNのバンドギャップEg（AlN）の大きさが6．2であることから（参考：Eg（InN）＝2．2eV<Eg（GaN））、$Al_xGa_{1-x}N$（$0<X<1$）のバンドギャップEg（$Al_xGa_{1-x}N$）は、これらEg（GaN）およびEg（AlN）を用いた次式で与えられ、

【0009】

$$Eg(Al_xGa_{1-x}N)=XEg(AlN)+(1-X)Eg(GaN)$$
$$=3.4+2.8X\ [eV]\ (0<X<1)$$

【0010】となる。したがって、AlGaNはGaNに比べて大きなバンドギャップを持ち、結晶結合力もより大きく、GaNを上回る高温・高耐圧動作が可能となる。

【0011】なお、以上の議論はGaAs系においても同様であるが、AlGaAsはGaAsに比べて電子移動度が著しく低下するため、高周波デバイスのチャネル材料として適当でない。それに対して、GaN系においてAlGaNの電子移動度は、GaNの電子移動度に比べて低下するものの許容範囲内（5～6割程度以上の移動度）の高い値である。ちなみに、本願発明者らによって、GaNおよび$Al_{0.1}Ga_{0.9}N$の室温電子移動度として、それぞれ350および170cm^2／Vsが観測されている。そのため、AlGaNをチャネル材料として用いることにより、GaAs系を用いた場合よりも高温・高耐圧動作が可能なデバイスを実現することができる。また、GaN系においてはGaAs系よりも強い結晶結合力が得られ、バンドギャップが大きくなり、耐振動特性および耐放射特性も向上する。

【0012】次に、本発明の具体的な適用例について説明する。図1は、本発明を適用したFETを示す断面図である。同図に示すように、SiC基板1上に$Al_{x0}G$＊＊$a_{1-x0}N$バッファ層2が形成され、その上に$Al_{x1}Ga_{1-x1}N$チャネル層3が形成され、その上にソース電極10、ゲート電極11およびドレイン電極12が形成され、これらによりFETが構成されている。なお、$0<X0\leqq1$，$0<X1<1$である。

【0013】図2は、本発明を適用したHFETを示す断面図である。同図に示すように、SiC基板1上に$Al_{x0}Ga_{1-x0}N$バッファ層2が形成され、その上に$Al_{x1}Ga_{1-x1}N$チャネル層3が形成され、その上に$Al_{x2}Ga_{1-x2}N$障壁層4が形成され、その上にソース電極10、ゲート電極11およびドレイン電極12が形成され、これらによりHFETが構成されている。なお、$0<X0\leqq1$，$0<X1<X2<1$である。本構造においては、デバイス動作に寄与する電子は$Al_{x2}Ga_{1-x2}N$障壁層4と$Al_{x1}Ga_{1-x1}N$チャネル層3との界面近傍のチャネル領域に集中的に存在する。

【0014】また、図1、2に示した構造に中間層を付加することにより、チャネル層等の結晶性を向上させることができる。図3は、図1の構造に中間層としてGaN層を設けた例を示す。同図に示すように、SiC基板1上に$Al_{x0}Ga_{1-x0}N$バッファ層2が形成され、その上に中間層としてGaN層5が形成され、その上にAl

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$Al_{x1}Ga_{1-x1}N$チャネル層3が形成され、その上にソース電極10，ゲート電極11およびドレイン電極12が形成され、これらによりFETが構成されている。なお、$0<X0\leqq1$，$0<X1<1$である。

【0015】図4は、図2の構造に中間層としてGaN層を設けた例を示す。同図に示すように、SiC基板1上に$Al_{x0}Ga_{1-x0}N$バッファ層2が形成され、その上に中間層としてGaN層5が形成され、その上に$Al_{x1}Ga_{1-x1}N$チャネル層3が形成され、その上に$Al_{x2}Ga_{1-x2}N$障壁層4が形成され、その上にソース電極10，ゲート電極11およびドレイン電極12が形成され、これらによりFETが構成されている。なお、$0<X0\leqq1$，$0<X1<X2<1$である。

【0016】ところで、上述したように図2および図4に示す窒化物半導体を用いたヘテロ構造電界効果トランジスタ（HFET）においては、ヘテロ界面に特有の正または負の分極電荷が発生する。HFETがチャネル電子の形成されるヘテロ界面以外にもヘテロ界面を有し、このヘテロ界面が正の分極電荷を誘起する場合には、このヘテロ界面に電子が引きつけられ、チャネル電子層以外にも電子層が形成される。このような非チャネル電子の存在は、HFETの低周波動作に影響を与えないものの、HFETの高周波特性を劣化させる。電子が走行するチャネル層直下の障壁として$Al_xGa_{1-x}N$層（$0<X<1$）が設けられている場合は、上述のような状況が起こり得る。そこで、HFETを高周波デバイスとして用いる場合には、非チャネル電子を消滅させることにより、高周波特性を向上させることができる。

【0017】図5は、電子が走行するチャネル層の直下に$Al_xGa_{1-x}N$層（$0<X<1$）が設けられたHFETを示す。同図に示すように、SiC基板101上に$Al_{x0}Ga_{1-x0}N$バッファ層102が形成され、その上に中間層としてGaN層105が形成され、その上に$Al_{x1}Ga_{1-x1}N$障壁層106が形成され、その上にGaNチャネル層103が形成され、その上に$Al_{x2}Ga_{1-x2}N$障壁層104が形成され、その上にソース電極110、ゲート電極111およびドレイン電極112が形成されている。なお、$0<X0\leqq1$，$0<X1<X2<1$，X1：一定である。

【0018】この構造は特願平10-56529号に開示されているものであり、電子が走行するGaNチャネル層の直下に$Al_xGa_{1-x}N$層（$0<X<1$）を設けたダブルヘテロ構造を用いることにより、チャネル内の2次元電子ガスの分布幅が縮小されてアスペクト比が向上し、相互コンダクタンス（gm）を増大させることができる。

【0019】図6は、図5の層構造におけるチャネル・ポテンシャル構造を2次元電子の分布とともに示したものであり、チャネル電子以外に副次的な2次元電子層が形成されている。この副次的な電子層の存在は、HFETの低周波動作に影響しないが、高周波特性の劣化原因となっている。そこで、以下に示す工夫により上述の副次的な電子層の発生を防ぐ。

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【0020】図7は、図5の構造に本発明を適用した層構造である。同図に示すように、SiC基板1上に$Al_{x0}Ga_{1-x0}N$バッファ層2が形成され、その上に中間層としてGaN層5が形成され、その上に$Al_{x1}Ga_{1-x1}N$障壁層6が形成され、その上にGaNチャネル層3が形成され、その上に$Al_{x2}Ga_{1-x2}N$障壁層4が形成され、その上にソース電極10、ゲート電極11およびドレイン電極12が形成されている。なお、$0<X0\leqq1$，$0<X1<X2<1$，X1：傾斜，$0<XA<1$，XBはほぼ0（$XB<0.05$）である。

【0021】本構造においては、電子が走行するGaNチャネル層の直下の$Al_xGa_{1-x}N$層が$Al_xGa_{1-x}N$層直下のGaN層とAl組成不連続を起こさないように、$Al_xGa_{1-x}N$層のAl組成Xに深さ方向に減少する傾斜を施し、GaN層とX＝0で接続されている。傾斜の付け方は、例えば図8に示すようなものが考えられる。

【0022】図8（a）～（f）は、$Al_xGa_{1-x}N$層のAl組成Xに施す深さ方向に減少する傾斜を示す。これらの図に示すように、Al組成X1の分布のさせ方には種々のバリエーションがある。少なくとも電子が走行するGaNチャネル層の直下の$Al_xGa_{1-x}N$層が$Al_xGa_{1-x}N$層直下のGaN層とAl組成不連続を起こさないように、$Al_xGa_{1-x}N$層のAl組成Xに深さ方向に減少する傾斜を施してやればよい。ただし、Al組成X1の分布が不連続な箇所においては、そのギャップΔXがΔX≦0.05となるようにする必要がある。なお、このような傾斜は$Al_xGa_{1-x}N$層を気相成長させる際に、Alを含むソースガスの供給を調整することによって容易に実施される。

【0023】図9は、図7において図8のAl組成変化を用いた場合のチャネル・ポテンシャル構造を2次元電子の分布とともに示す。チャネル電子の存在するヘテロ界面以外にはポテンシャル・プロファイルの不連続とそれに伴う分極電荷の発生および電子の発生が消滅する結果、チャネル電子のみが存在し、図に示すような副次的な2次元電子層の形成が解消されている様子が示されている。このように本発明によってHFETの高周波特性を向上させることができる。なお、GaNチャネル層を$In_yGa_{1-y}N$チャネル層（$0<Y\leqq1$）に置き換え、また$Al_zGa_{1-z}N$チャネル層（$0<Z\leqq1$，$Z<X1$，$Z<X2$）と置き換えても上記同様の効果が得られる。

【0024】以上においては、基板材料としてSiCを用いたが、本発明はこれに限られるものではない。例えばサファイア基板またはGaN基板を用いてもよい。その場合、$Al_{x0}Ga_{1-x0}N$バッファ層2におけるAl組

成X0を0≦X0≦1にする必要がある。

【0025】

【発明の効果】以上説明したとおり本発明は、窒化物半導体を用いたFETまたはHFETの高温動作における信頼性の向上、耐熱性の向上、耐圧の増加を実現することができる。また、耐振動特性および耐放射線特性の向上も実現できる。さらに、チャネル層の直下に設けられた$Al_xGa_{1-x}N$層（0<X<1）に副次的電子層が発生することを防止することができ、HFETの高周波特性を向上できる。

【図面の簡単な説明】

【図1】 本発明の一つの実施の形態（FET）を示す断面図である。

【図2】 本発明のその他の形態（HFET）を示す断面図である。

【図3】 図1の構成にGaN層付加した様子を示す断面図である。

【図4】 図2の構成にGaN層付加した様子を示す断面図である。

【図5】 特願平に開示されている断面図である。

【図6】 図5におけるチャネル・ポテンシャル構造を示す説明図である。

【図7】 本発明のその他の形態（HFET）を示す断面図である。

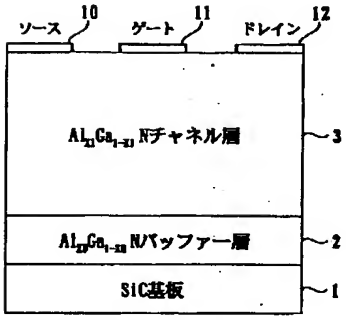
【図8】 図7におけるAl組成の傾斜例を示す説明図である。

【図9】 図7におけるチャネル・ポテンシャル構造を示す説明図である。

【符号の説明】

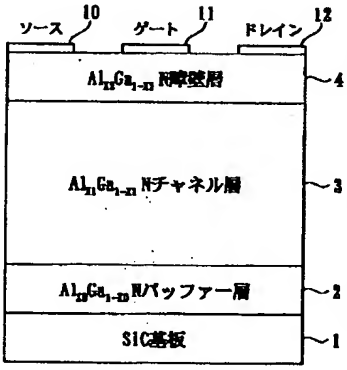
1…SiC基板、2…$Al_{X0}Ga_{1-X0}N$バッファ層、3…$Al_{X1}Ga_{1-X1}N$チャネル層、4…$Al_{X2}Ga_{1-X2}N$障壁層、5…GaN層、10…ソース電極10、11…ゲート電極、12…ドレイン電極。

【図1】



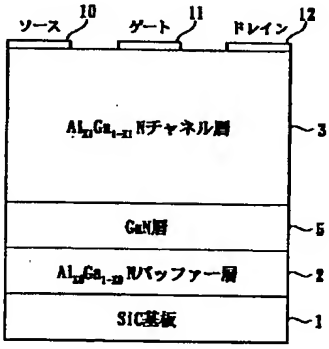
0<X0≦1，0<X1<1

【図2】



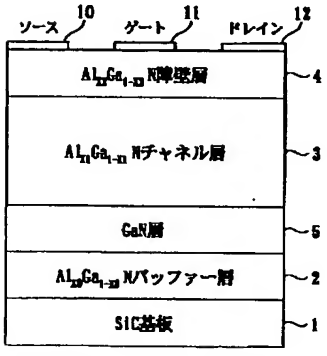
0<X0≦1，0<X1<X2<1

【図3】



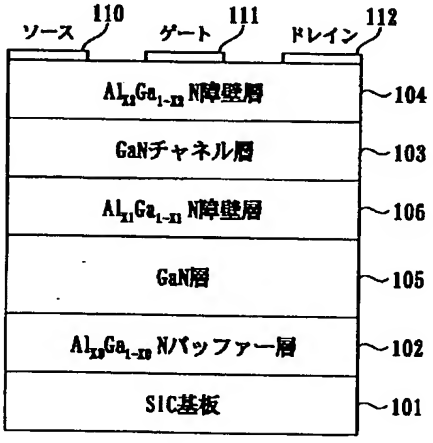
0<X0≦1，0<X1<1

【図4】



0<X0≦1，0<X1<X2<1

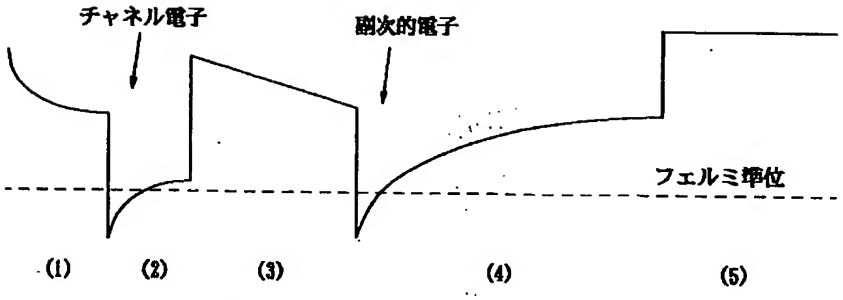
【図5】



0<X0≦1，0<X1<1

X1：一定

【図6】



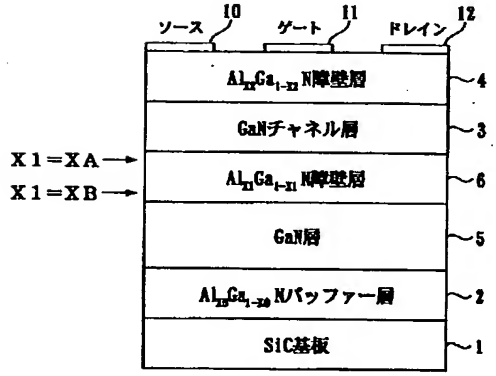
(1)$Al_{X2}Ga_{1-X2}N$障壁層　　(4)GaN層

(2)GaNチャネル層　　(5)$Al_{X0}Ga_{1-X0}N$バッファー層

(3)$Al_{X1}Ga_{1-X1}N$障壁層(X1:一定)

$0<X0\leqq1$，$0<X1<1$，$0<X2<1$

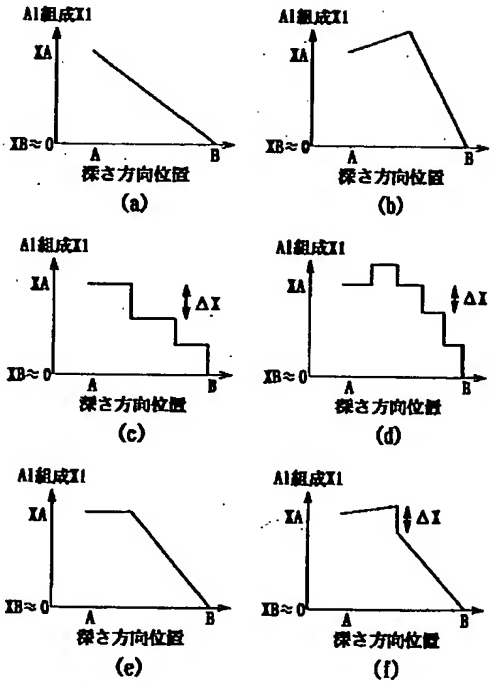
【図7】



$0<X0\leqq1$，$0<X1<X2<1$

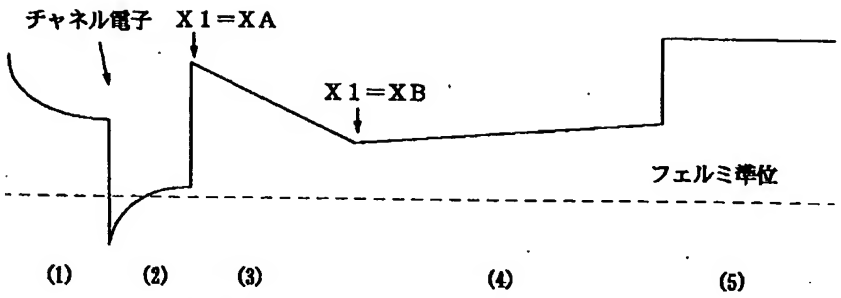
X1：傾斜，$0<XA<1$，$XB\approx0$ ($XB<0.05$)

【図8】



$XB\approx0$ ($XB<0.05$)，$\Delta X\leqq0.05$

【図9】



(1)$Al_{X2}Ga_{1-X2}N$障壁層　　(4)GaN層

(2)GaNチャネル層　　(5)$Al_{X0}Ga_{1-X0}N$バッファー層

(3)$Al_{X1}Ga_{1-X1}N$障壁層（X1：傾斜，$0<XA<1$，$XB\approx0$（$XB<0.05$））

$0<X0\leq1$，$0<X1<1$，$0<X2<1$

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Reproducibility of growing AlGaN/GaN high-electron-mobility-transistor heterostructures by molecular-beam epitaxy

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Abstract

High-quality GaN/AlGaN high-electron-mobility transistors (HEMT) characterized by room temperature mobilities of ~1000 $cm^2 V^{-1} s^{-1}$ and sheet electron densities in the range of 3×10^{12}–2×10^{13} cm^{-2} have been grown by reactive molecular-beam epitaxy on insulating C-doped GaN template layers. Growth data and mobility values resulting from over 50 HEMT growth experiments on 2 in. diameter sapphire wafers are presented to show the remarkable overall high yield and reproducibility of the HEMT structures grown by this method. The use of insulating C-doped GaN buffer layers has greatly increased reproducibility of the device structures by ensuring device isolation through controlled carbon doping. Moreover, an undoped GaN channel layer of remarkably low defect density and high mobility can be grown on the C-doped GaN template with high reproducibility. Precise control of the growth temperature was key to achieving the high quality and reproducibility of the structures.

1. Introduction

Two-dimensional electron systems formed by AlGaN/GaN heterostructures are considered highly promising for high power and high frequency electronic applications owing to the robust material stability and ideal electron transport properties. Material quality of the III-nitride semiconductors has been substantially improved in recent years using the growth techniques metal-organic chemical vapor deposition (MOCVD), hydride vapor-phase epitaxy (HVPE) and molecular-beam epitaxy (MBE). This has led to frequent reports of record-breaking mobility values now above 10^4 $cm^2 V^{-1} s^{-1}$ at low temperatures for both MBE and MOCVD grown two-dimensional electron gas (2DEG) structures [1–4]. In the meantime, GaN high-electron-mobility-transistor (HEMT) devices fabricated from high-quality MBE and MOCVD grown layers have demonstrated significant performance in power output, frequency limit, and noise level [5–8].

Growth reproducibility and yield will be an essential element in the event of scaling up for potential commercial production of AlGaN/GaN HEMT devices and circuits. However, there have been very few data or discussions dealing with the reproducibility issue in the literature. In this article, we will examine the reproducibility status in the growth of high-quality GaN HEMT structures using ammonia MBE. Two major factors pertinent to reproducibility and yield will be addressed here. The first important factor is the reproducible growth of the insulating, thick GaN buffer in the HEMT structure, which is necessary for achieving device isolation as well as good rf performance. Any irreproducibility in achieving high resistivity of this thick buffer layer will directly affect the yield of working devices. The second measure of growth reproducibility is the quality of the 2DEG, for which mobility is generally a good

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criterion. The electron mobility is a sensitive measure of interface and overall material quality and directly affects the speed and overall performance of the HEMT devices.

Growth and mobility data resulting from about fifty growth experiments for HEMT structures will be examined statistically to assess yield and reproducibility, and to look for trends that link quality and reproducibility, to key growth conditions. The impact of some important growth conditions, such as carbon doping of the thick buffer layer and the optimal growth temperature, will be discussed.

2. Experimental conditions

Growth of GaN epilayers and HEMT structures was performed with a custom-built MBE system equipped with an additional UHV magnetron sputter epitaxy capability. Magnetron sputter epitaxy was employed for depositing a thin (~200 Å) AlN nucleation buffer layer, which was then followed by the MBE growth of the GaN epilayers or HEMT structures. Ammonia was used as the nitrogen source and its flow rate was controlled in the range of 1–140 sccm by an electronic mass-flow controller. DC reactive sputter deposition of the AlN nucleation layer was carried out using a high purity Al target, 50 W power, 15 sccm ammonia, and 40 sccm of Ar, at a substrate temperature of 880°C. For the MBE growth, ultra-high purity Ga (99.999999%) and Al (99.9999%) were used for the effusion sources. Silane was used as the silicon dopant source. Methane was used as the carbon dopant source, and a low-energy saddle-field ion source was used to crack the methane and achieve effective carbon incorporation. Substrates were 2 in. diameter sapphire wafers back coated with heat absorbing Mo coatings. Growth temperature was measured by a pyrometer with emissivity set to 0.7. Growth rate was monitored using in situ laser reflectometry.

Hall-effect measurements were performed on 5 × 5 mm size samples using the Van der Pauw geometry. Photoluminescence spectra were measured with a He–Cd laser as the excitation source while X-ray diffraction characterization was performed using a Phillips high-resolution triple-axis diffractometer.

3. Reproducible growth of the insulating buffer layer

Native nitrogen vacancies and residual impurities such as silicon and oxygen lend a strong tendency of n-type autodoping to GaN epitaxial materials. The background doping concentration is typically higher than 1×10^{16} cm^{-3}, even under optimal growth conditions. One way of neutralizing these background electrons in order to achieve highly resistive material is to modify certain structural defects such as dislocations and grain boundaries. Certain defects or defect–impurity complexes are acceptor-like, thus compensating or trapping electrons [9–11]. Irreproducibility arises, however, because the nature and densities of the structural defects are difficult to control in typical growth experiments. In the case of ammonia MBE growth, lowering the growth temperature can generally introduce acceptor-like defects, which lead to more resistive films. Table 1 summarizes some results from our growth experiments aimed to look at the effects of different growth temperatures, which revealed this trend. Reducing the growth temperature by 50–100°C from the ideal temperature used for high mobility materials, caused an increase in resistivity accompanied by broadening of the X-ray rocking curve width, and a reduction in the intensity of the band-edge emission relative to the yellow luminescence. In addition, a lower ammonia flux appeared to be more favorable for achieving higher resistivity when growing at lower than optimal temperatures, as can be seen from the comparison of the third and fourth samples in Table 1. However, the resistivities of the intentionally undoped GaN layers grown at low temperatures, were far from being reproducible or sufficiently high for HEMT applications.

On the other hand, carbon doping provides an excellent solution to the reproducible growth of the insulating buffer layers, as well as for the high-quality HEMT. Carbon atoms substituting nitrogen sites create deep acceptor centers in GaN [12,13] and thus can provide the necessary compensation for the residual and native donors in GaN epilayers. Using a methane flow rate of 1–2 sccm and an anode voltage of 800 V for the ion source, we achieved carbon incorporation in the GaN epilayers at concentrations in the low to mid-10^{18}

Table 1
Effect of growth temperature and carbon doping on resistivity and other properties of GaN films grown by ammonia MBE

Sample	Growth temperature (°C)	NH_3 (sccm)	Resistivity (Ω cm)	X-ray ω scan FWHM (″)	PL intensity ratio (band-edge/yellow)
Undoped GaN	900	50	0.078	303	39
Undoped GaN	850	6	30.7	538	21.6
Undoped GaN	790	6	516	576	5.6
Undoped GaN	790	50	1.5	560	1.4
C-doped GaN	900	50	10^8	573	0.14

cm^{-3} range as measured by secondary ion mass spectroscopy (SIMS). These values were higher than the usual background donor concentrations. Ionization of the methane gas was found necessary to achieve any detectable incorporation of carbon into the growing films [14]. The fact that neutral methane does not result in carbon incorporation is an advantage, in that there is essentially no memory effect with this dopant gas. The C-doped GaN epilayers were extremely resistive with resistivities generally higher than 10^8 Ωcm. The growth of insulating C-doped GaN is highly reproducible, and does not require any reduction in growth temperature. In fact the ideal temperature for growing C:GaN was the same as that used for growing high mobility GaN layers, i.e. 900°C at ammonia flow rate of 50 sccm.

Broadening of the X-ray rocking curve FWHM and quenching of the band-edge exciton emissions were observed in the C-doped GaN layers (see Table 1). It is not excluded that structural defects caused by ionic effects have also contributed to the compensation of residual donors in the films. However, structural defects alone do not provide reliable or sufficient compensation for electrons, because many of the structural defects such as dislocations and grain boundaries could be both a source of compensating centers, and at the same time a ghetto for unwanted impurity and native donors. The role of carbon as a deep acceptor center is still essential in ensuring total compensation of all electrons in the MBE grown GaN films.

4. Reproducible growth of the high-quality channel layer

Although the insulating C-doped GaN technique provided the basis for a reproducible, high-yield approach to MBE-grown GaN HEMTs, another crucial step was the ability to grow a thin, high-quality, nominally undoped GaN channel layer on the insulating buffer layer, since the latter contains a high level of compensation and is not suitable for use as the channel material. Our experiments demonstrated that such channel layers could be grown with excellent material quality and surprisingly high reproducibility.

The Hall-effect measurement shown in Fig. 1 indicate excellent transport properties of a 4000 Å, silicon-doped, GaN channel layer grown on a 2 μm thick C:GaN buffer layer. The carrier density is in the 10^{16} cm^{-3} range, and shows a well-defined thermally activated dependence on temperature, a behavior typical of bulk, non-degenerate semiconductors. The bulk (three-dimensional) electron mobility in the channel layer is 470 $cm^2 V^{-1} s^{-1}$ at room temperature, and the peak value is over 1000 $cm^2 V^{-1} s^{-1}$. Photoluminescence measurements revealed intense excitonic emissions from the channel layer in contrast to the quenched band-edge emissions in the C-doped buffer layer. This indicates that there was very little

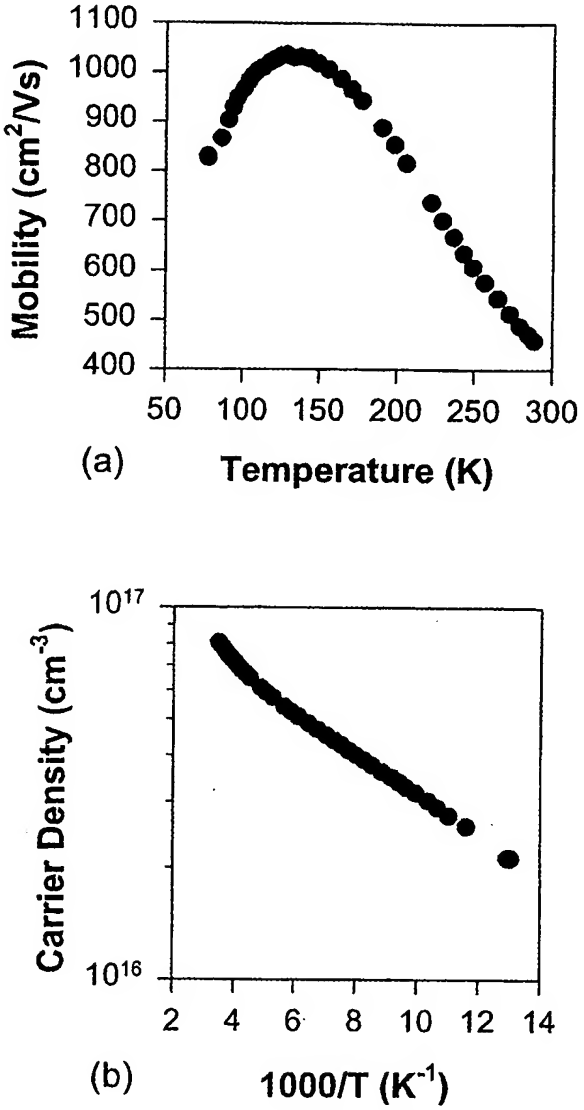

Fig. 1. (a) Temperature-dependent Hall mobility, and (b) carrier density measured of a 4000 Å thick, Si-doped GaN channel layer grown on an insulating C-doped GaN template.

memory effect of the carbon species when the growth proceeded from the C-doped buffer to the channel layer. TEM studies also confirmed that the channel layer had much fewer threading dislocations than the underlying buffer layer.

The high-quality channel layer proved to be very reproducible provided that the growth temperature was precisely controlled. For most growth experiments, the ammonia flow rate was set to 50 sccm, while the material quality was optimized via the growth temperature. We found that as the growth temperature was raised, the growth rate remained constant up to 880°C, above which the growth rate began to decrease rapidly,

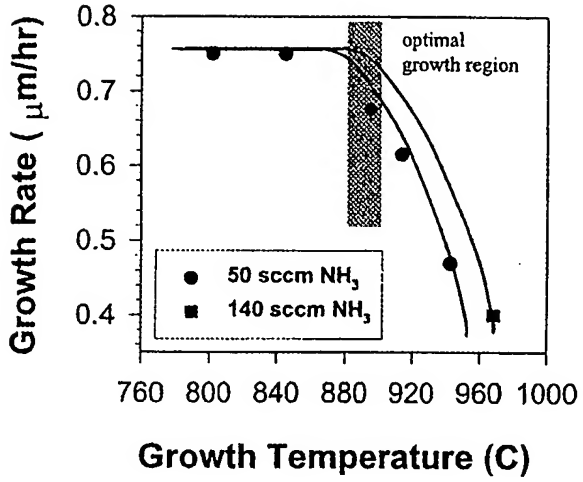

Fig. 2. Effect of growth temperature on growth rate for GaN grown by ammonia MBE. The shaded area marks the temperatures range ideal for achieving optimal growth quality and high mobility.

reaching zero at 960°C, as shown in Fig. 2. The temperature range for growing the high-quality GaN layers was found to be very narrow, only about 10–20°C, and coincided with the onset of the rapid growth rate decline, as indicated in Fig. 2. For layers grown just slightly below this temperature range, a significant drop in crystalline quality as well as electron mobility was observed. Growth at temperatures higher than that, on the other hand, led to hazy, rough films usually with reduced electron mobility.

The decline of growth rate at high temperatures was due to increased desorption of both Ga and N, but most importantly N, from the film surface. According to the findings of some recent studies [15,16], the desorption rate of N increases with temperature much more rapidly than does that of Ga. Thus with increasing temperature the growth process quickly becomes deficient in nitrogen and the growth rate starts to be limited by the nitrogen supply. The data in Fig. 2 showed evidence for this trend. At 960°C, the growth rate dropped to zero when a 50 sccm ammonia flow rate was used, but again increased to 0.4 $\mu m\,h^{-1}$ at this temperature after the ammonia flow rate was increased to 140 sccm. This clearly indicates that the growth rate was limited by the nitrogen supply at this elevated temperature. At the temperature where the growth rate begins to drop, however, the ratio of the Ga desorption rate to the N desorption rate becomes similar to the III/V ratio in the supplying fluxes, leading to the balanced, near equilibrium growth condition described in recent modeling work on GaN growth [16]. This is probably why this temperature was optimal for the growth of the high-quality channel layers.

With in situ monitoring of the growth rate using a laser reflectance setup, we have been able to control the growth temperature in the very tight range discussed above, and have achieved high reproducibility of the channel layers grown on C-doped GaN buffer layers.

5. Mobilities of the high-electron-mobility-transistor structures

Following the growth of the insulating GaN buffer layer and the undoped GaN channel layer as described in the preceding sections, an HEMT structure was completed by the subsequent growth of a barrier layer of the larger band gap AlGaN. The HEMT structures grown using this approach demonstrated excellent electrical properties, high yield and reproducibility.

Fig. 3 gives an example of the excellent electrical properties of an HEMT structure grown with 2 μm C:GaN buffer, 2000 Å GaN channel, and 130 Å AlGaN. The sheet carrier density measured by Hall effect was almost constant with temperature as shown in Fig. 3(a), indicating the existence of a 2DEG and the absence of other parallel conduction paths. The room temperature mobility was 1284 $cm^2\,V^{-1}\,s^{-1}$. The mobility at 77 K was 7120 $cm^2\,V^{-1}\,s^{-1}$ for a sheet electron density of 3.9×10^{12} cm^{-2} as measured.

Over the last year, we have performed about 50 growth experiments for the HFET structures using the approach outlined here. Fig. 4 presents a statistical summary of the room temperature mobilities of the 50 HEMT structures grown. About 75% of the growth experiments yielded electron mobilities higher than 800 $cm^2\,V^{-1}\,s^{-1}$. This yield of high mobility structures is quite satisfactory considering that the statistics shown include samples of various structures and prepared un-

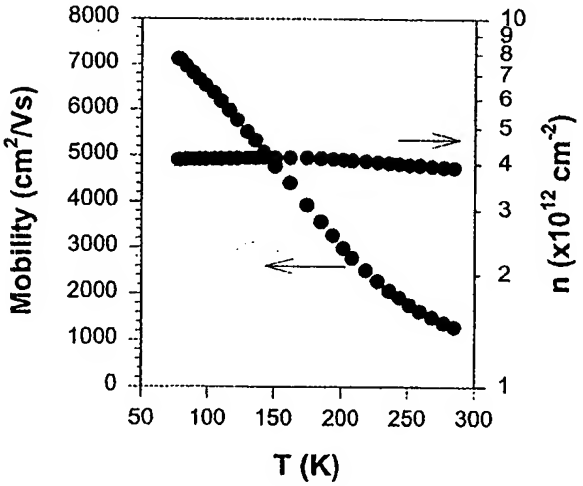

Fig. 3. Temperature-dependent Hall-effect data measured from a high quality HEMT structure grown with 2 μm C:GaN buffer, 2000 Å GaN channel, and 130 Å AlGaN.

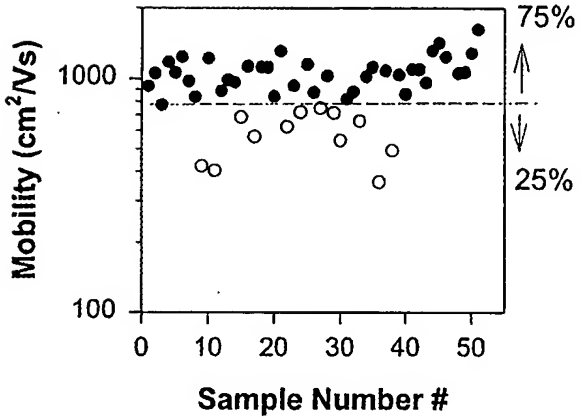

Fig. 4. Statistics of room temperature mobility of all 50 GaN HFET structures grown by ammonia MBE over one year period. The dashed line separates the samples with mobilities over 800 $cm^2 V^{-1} s^{-1}$ from those with lower mobilities.

der different growth conditions. These also include failed HEMT structures grown under, what was later found to be grossly off-ideal conditions. This indicates that the growth technique is quite robust and error tolerant.

The thickness of the C:GaN buffer was kept at 1.5–2.0 μm. The channel layer thickness was 2000 Å for most samples, but thicker channels of up to 4000 Å were used for some samples. The thickness of the AlGaN layer was varied between 80 and 500 Å, although a typical thickness of 150 Å has been used for the majority of the samples. The Al concentration in the barrier was varied between 8% and 50%. The AlGaN barrier was doped with silicon only for some of the samples. In most samples, the AlGaN layer was not intentionally doped, and the 2DEG was formed primarily due to the piezoelectric and spontaneous polarization effects.

The HEMT samples with too high Al concentration (>40%) in the barrier and with barrier thickness greater than 200 Å were prone to relaxation of the pseudomorphic strain between GaN and AlGaN, which could lead to significant degradation of the 2DEG and dramatically reduced electron mobility. Preventing such an overshoot in the Al concentration depends on good control of the Al flux, which was complicated by the strong tendency of Al creeping out from its crucible under the high ammonia environment. To resist the Al creeping problem, specially designed Al cells with water-cooled lips proved to be quite effective and resulted in a better control of the Al flux.

Doping the AlGaN barrier with silicon (to 10^{18}–10^{19} cm^{-3} level) also resulted in a slight decrease in room temperature mobility, typically 10–20% as observed. A doped AlGaN barrier is sometimes preferred for achieving a low contact resistance at the source and drain of the HFET.

Table 2
Mobility and carrier density values for five consecutively grown GaN HEMT samples with nominally identical sample structure and growth conditions

HEMT no.	n_s ($\times 10^{13}$ cm^{-2})	μ ($cm^2 V^{-1} s^{-1}$)
1	1.58	980
2	1.52	958
3	1.60	976
4	1.48	1008
5	1.51	1016

Run-to-run reproducibility of nominally identical HEMT structures has also been tested. Five consecutive growth runs aimed at reproducing the same HEMT structure under nominally identical growth conditions have been performed, and yielded very uniform mobility and sheet carrier density values with quite small scatter from run to run. The growth structure aimed for consists of 2 μm C-doped insulating GaN buffer layer, 2000 Å GaN channel layer, and an $Al_{0.3}Ga_{0.7}N$ layer comprising of 40 Å spacer region, 40 Å cap region, and 60 Å donor region doped with Si to 5×10^{18} cm^{-3}. The measured mobility and sheet carrier density data are given in Table 2. From these five growth runs, the scatter in the electron density values was less than 7.5%, and the variation in the electron mobility values was within 5.7%.

A consistent correlation between mobility and sheet carrier density was observed in these HEMT samples. Fig. 5 shows the μ vs. n data for all the high mobility samples, while low mobility samples resulting from non-ideal or failed growth are excluded in order to reveal the trend. The room temperature mobility showed a small but consistent decrease with increasing carrier density (Fig. 5a). The trend was more dramatic for the mobility measured at 77 K. As shown in Fig. 5b, the 77 K mobility was substantially higher in samples with low sheet carrier densities than in samples with high sheet densities. Such a trend indicates that the AlGaN layer was an important source of scattering in these structures, since the density of the 2DEG corresponds to the same density of parent donors in the AlGaN layer. In addition, the density of the 2DEG was found to correlate closely with the Al concentration in the AlGaN barrier, indicating the 2DEG was largely induced and confined by the piezoelectric field. A larger Al concentration in the AlGaN layer leads to larger alloy disordering, a higher density of interface charges, larger potential fluctuation at interface due to roughness, and thus causes a lower mobility. At higher sheet carrier densities, the 2DEG will also be confined closer to the interface, thus more exposed to scattering by interface roughness, interface charge (piezoelectric) and alloy disorder [17,18]. Therefore, improving the quality of the AlGaN layer and the interface smoothness is paramount to achieving even higher electron mobility in these HEMT structures.

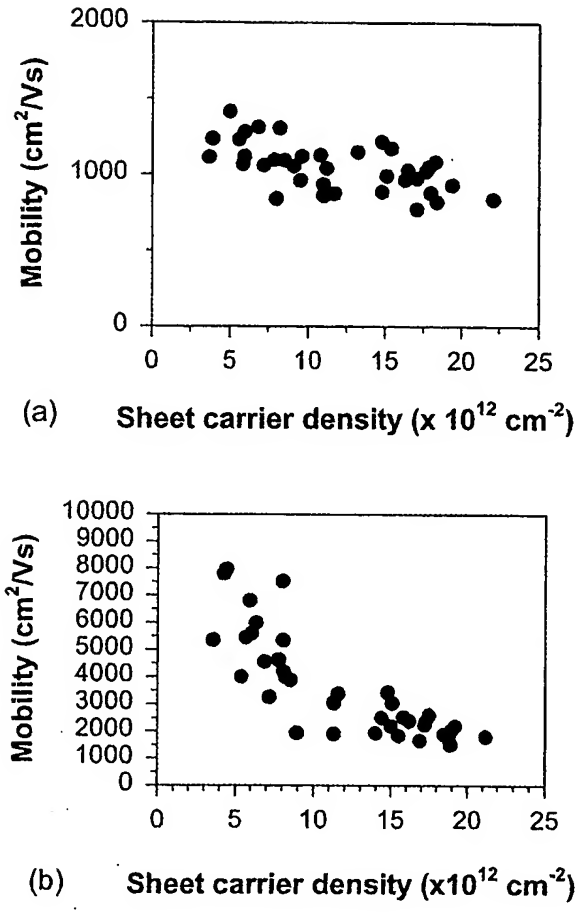

Fig. 5. Two-dimensional electron mobility vs. electron sheet density, (a) at room temperature, and (b) at 77 K, for GaN HFET structures grown by ammonia MBE.

Devices fabricated from these wafers showed very good yield and consistency. Excellent device characteristics both in DC and rf mode have been obtained. The device results will be reported elsewhere.

6. Conclusion

The growth of high-quality GaN HEMT structures by reactive MBE using an approach emphasizing high yield and reproducibility has been described in detail. Several key growth conditions necessary for achieving reproducible high-quality results have been determined. [illegible] the ability to grow reproducibly a thin channel layer of high material quality provided the basis for achieving high mobility 2DEGs desirable for HEMT devices. Growth temperature was found to be a key, sensitive growth parameter that needed precise control. The optimal growth temperature was determined to be at the onset of growth rate decline due to accelerated thermal decomposition at high temperature. The mobilities of the HEMT structures showed a consistent decline with increasing carrier density, especially at cryogenic temperatures.

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Growth of high-performance GaN modulation-doped field-effect transistors by ammonia-molecular-beam epitaxy

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The growth of AlGaN/GaN modulation-doped field-effect transistors (MODFETs) by ammonia-molecular-beam epitaxy on sapphire substrates is reported. C-doped GaN (2 μm thick) was used as the insulating buffer layer in the device structures. The MODFET structure was completed by the subsequent growth of 2000 Å of undoped GaN as the channel layer and 130 Å of $Al_xGa_{1-x}N(0.1 \leq x \leq 0.3)$ as the donor barrier layer. Sheet carrier densities of up to $2 \times 10^{13}\,cm^{-2}$ with mobility of $\sim 1000\ cm^2/Vs$ have been achieved even without doping the $Al_xGa_{1-x}N$ barrier, indicating a large piezoelectric effect and excellent interface quality. The MODFET layers grown exhibited a unique surface morphology showing very flat plateaus with rms roughness of 0.8 nm on the plateaus and rms roughness of 8 nm over a larger area. A 100-μm-wide device with a 1 μm gate length exhibited a maximum dc current drive of 0.9 A/mm, a peak transconductance of 160 mS/mm, a current gain cutoff frequency of 15.6 GHz, and a maximum oscillation frequency of 49.4 GHz. The high dc and rf performance is attributed to the high two-dimensional electron mobility, high sheet charge density, and insulating property of the C-doped GaN buffer. [S0734-2101(00)05402-6]

I. INTRODUCTION

AlGaN/GaN modulation-doped field-effect transistors (MODFETs) are an ideal candidate for high-power and high-frequency applications. Compared with GaAs, GaN has a greater electron saturation velocity, a higher breakdown field, and much higher thermal and chemical stability.[1] Moreover, due to a larger conduction-band discontinuity at the GaN/AlGaN interface, it is possible to achieve a two-dimensional (2D) electron gas with a sheet carrier density much higher than in conventional III–V heterostructures. In the last few years, the performance of GaN MODFETs has been rapidly advanced to a state-of-the-art level. The success includes setting new records of microwave power capability in the *S*, *X*, and *K* band,[2–4] and achievement of a current gain cutoff frequency of >50 GHz, and a power gain cutoff frequency of >100 GHz.[5–7]

GaN/AlGaN MODFETs with promising dc and rf performance have been demonstrated using both the metal–organic chemical-vapor deposition (MOCVD) and molecular-beam epitaxy (MBE) growth techniques.[2–9] The growth of such device structures presented a number of challenges. One critical issue is the growth of a thick semi-insulating GaN buffer layer. The thick buffer is necessary so that the channel area is well separated from the defective GaN/substrate interface. As well, an insulating buffer is essential for low-loss, high-performance rf devices. To date, very little data have been reported on how to grow highly resistive GaN layers. A second issue is the electron mobility which has a direct impact on the frequency response of the devices. Earlier works on MBE-grown GaN MODFETs reported a relatively low mobility for a 2D electron gas. Recently, however, an AlGaN/GaN 2D electron gas grown by MBE with mobility comparable to the record values set by the MOCVD technique has been reported, underscoring the potential of the MBE technique for developing GaN power and high-speed devices.[10–12]

In this article, we report on the growth of AlGaN/GaN MODFETs by ammonia MBE using the C-doped GaN buffer layers. High 2D electron mobilities of $>1000\ cm^2/Vs$ and high sheet carrier densities up to $\sim 2 \times 10^{13}\,cm^{-2}$ were obtained for the heterostructures grown by this approach. The electrical measurement data and surface morphology of the MODFET layers are presented. MODFETs have been fabricated using photolithography to achieve a gate length of about 1 μm. The devices exhibited very promising rf performance even at this relatively large gate length.

II. EXPERIMENT

The growth system used in this study was a molecular-beam epitaxy/magnetron sputter epitaxy (MBE/MSE) dual-mode system. The MSE technique has been found to be a suitable technique to deposit a thin AlN nucleation layer for the heteroepitaxy of GaN on sapphire, and has been employed in achieving a record high bulk mobility of MBE-grown GaN.[13] A technique of carbon doping to obtain highly resistive GaN was also developed.[10] Methane gas injected into a saddle field ion gun was used for the carbon dopant source. It was discovered that cracking of methane by the ion source was needed to obtain sufficient carbon

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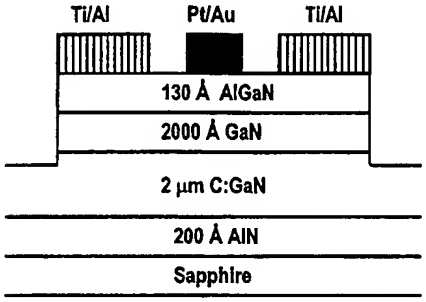

FIG. 1. Schematic structure of the AlGaN/GaN MODFETs grown by ammonia-MBE.

incorporation.[10] The ion source provides a low-energy ion flux with kinetic energy controllable by an anode voltage between 0 and 1000 V.

The layer structure of the MODFETs grown is illustrated in Fig. 1. 2 in. sapphire wafers were back coated with molybdenum to facilitate radiation heating as indium-free substrate mounting was employed. The sapphire substrate was degreased in chloroform for 15 min, dipped in $HF:H_2O$ (1:10) for 1 min, and rinsed in DI water for 10 min before being dried and loaded into the growth system. Nitridation of the sapphire surface was performed at 1000 °C and 100 sccm ammonia. The growth sequence was as follows. First, a 200 Å AlN nucleation layer was deposited at 880 °C by MSE under 40 sccm Ar and 15 sccm ammonia. Then, a 2-μm-thick, C-doped GaN layer was grown at 910 °C by MBE using 50 sccm ammonia and 950 V anode voltage for a methane flow of 1 sccm, followed by 2000 Å of undoped GaN and 130 Å of AlGaN using the same growth parameters of temperature and ammonia flow rate. Note that all temperature values in this article were measured with a pyrometer with emissivity set to 0.3. The growth rate for the C-doped GaN was 1 μm/h. During the growth of the channel layer, the growth rate was ramped from 1 to 0.5 μm/h.

Large sheet carrier densities were measured even without intentional doping of the AlGaN barrier, indicating a strong piezoelectric effect. The nominal Al fraction in the barrier was varied between 10% and 30% for the samples studied. The nominal values of the Al fraction were estimated from the respective AlN and GaN growth rates.

The MODFET layers were characterized by Hall-effect measurements using a Van der Pauw geometry with an applied field of 3 kG on 5×5 mm samples with soldered indium Ohmic contacts.

The processing of MODFET devices from these layers is reported in detail in another article.[14] Mesa isolation was achieved with chemically assisted ion-beam etching. Ohmic contacts on the source and drain were a Ti/Al 300 Å/800 Å double stack, annealed at 900 °C for 30 s in nitrogen. For the gate Schottky contacts, 300 Å of sputtered Pt backed up with 1000 Å/2000 Å of e-beam evaporated Pt/Au was used.

III. RESULTS AND DISCUSSION

The C-doped GaN layers grown using 1 sccm methane and 950 V extraction voltage exhibited high resistivities in the range of $10^6-10^7\,\Omega$ cm, as measured by the van der pauw method using high impedance electrometers. Secondary ion mass spectroscopy analysis found $\sim 1\times10^{18}\,cm^{-3}$ C in these layers.

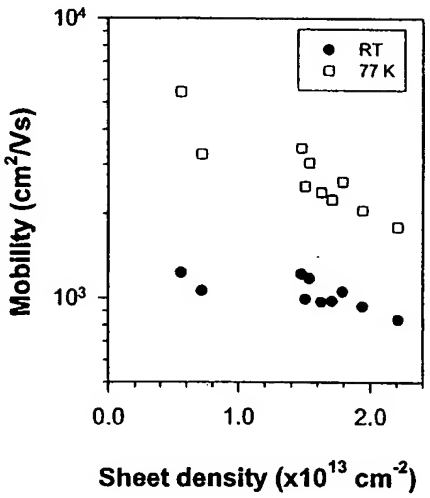

FIG. 2. Room-temperature and 77 K mobility against sheet carrier density for a series of AlGaN/GaN MODFET structures with undoped AlGaN barriers grown on sapphire (0001) substrates.

In Fig. 2, the room-temperature (RT) and 77 K mobilities are plotted against sheet carrier densities for a series of MODFET structures grown with different carrier densities. The highest sheet carrier density is about $2\times10^{13}\,cm^{-2}$ achieved in samples with 30% Al in the AlGaN barrier, which is slightly higher than most other reported values in the literature. The RT temperature mobility shows only a slight decrease with increasing carrier density. The RT mobility is maintained at $\geq 1000\,cm^2/V\,s$ for carrier densities up to $1.8\times10^{13}\,cm^{-2}$. The high mobility at RT is important for the speed of the devices operating at room temperature. The mobility at 77 K, however, shows a more sensitive dependence on carrier density. It increases significantly when the carrier density decreases from 2×10^{13} to $5\times10^{12}\,cm^{-2}$.

The layers with high sheet carrier densities ($\sim 2\times10^{13}\,cm^{-2}$) were used for device fabrication to achieve high-power and high-frequency performance. Figure 3 shows the temperature-dependent Hall mobility and carrier density for such a sample. The nearly constant carrier density as a function of temperature confirms no parasitic conduction in the C-doped buffer. The monotonic increase of mobility with decreasing temperature is another indication of the modulation doping where the 2D electron gas is spatially separated from the donor ions.

The MODFET layers exhibited an interesting surface morphology. Figure 4 shows the atomic force microscopy (AFM) image of the surface of the sample studied in Fig. 3. The AFM picture reveals grains about 0.5 μm in size with extremely flat tops. The overall roughness (rms) is 8 nm, however, the rms roughness on the flat plateau is only 0.8 nm. We believe the surface flattening of the layer occurred during the growth of the 200-nm-thick channel layer, where the growth rate was ramped from 1 to 0.5 μm/h. High tem-

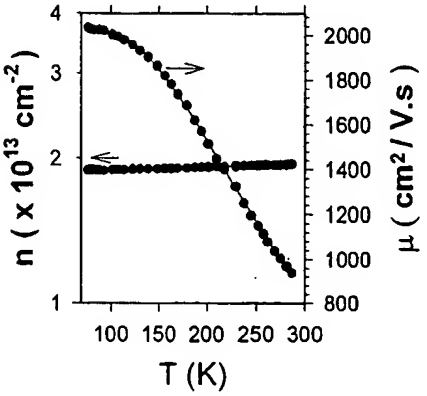

FIG. 3. Temperature dependence of Hall-effect mobility and sheet carrier density for an AlGaN/GaN MODFET layer used for fabricating devices of high-frequency and high-power capacities.

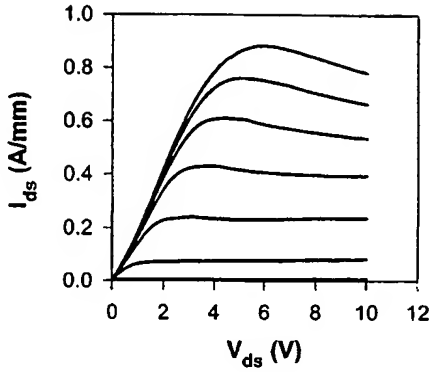

FIG. 5. Drain I–V characteristics of a device fabricated from the MODFET layer in Fig. 3 with a 1 μm gate length, and two gate fingers with a total width of 100 μm. The gate bias was swept from 1 to −5 V in steps of −1 V.

perature and small growth rate seem to promote the two-dimensional growth leading to the very flat plateaus. It would be extremely desirable if the atomically flat area can be extended to fill the whole surface area. Work is being done to further enhance the surface smoothness.

The devices fabricated from the MODFET layer in Fig. 3 exhibited very good dc and rf characteristics. Figure 5 shows the dc drain output characteristics measured on a device with a two finger ×50-μm-wide design and a measured gate length of 1 μm. The measured I–V output characteristics with V_{ds} set to 10 V exhibited a pinch-off voltage of −5 V and a peak transconductance of 160 mS/mm. A maximum drain current of 0.9 A/mm was also measured. The ability to achieve such high drain current densities is attributed to the high sheet charge density of the 2D electron gas. The negative differential output conductance observed at high drain current is due to self-heating in the channel, as the sapphire substrate is not a good thermal conductor. The heating problem could be largely relieved by using SiC substrates.[5,7]

The rf characterization of this device at room temperature showed a current gain cutoff frequency (f_T) of 15.6 GHz, and a maximum oscillation frequency (f_{max}) of 49.4 GHz. These are excellent rf characteristics considering the relatively large gate length (1 μm) used. The excellent rf performance is attributed to the high mobility and high density of the 2D electron gas, and also to the semi-insulating property of the C-doped GaN buffer. A conducting buffer layer not only will cause leakage current but also can induce parasitic capacitance that could degrade the rf performance. In fact, the drain-to-source capacitance for this device was found to be as low as 8×10^{-18} F/μm^2. This confirms the C-doped GaN is extremely resistive.

Full details of the rf performance characterizations at a range of temperatures are published elsewhere.[15] To obtain maximum rf performance, e-beam lithography will be required to achieve a much smaller gate length.

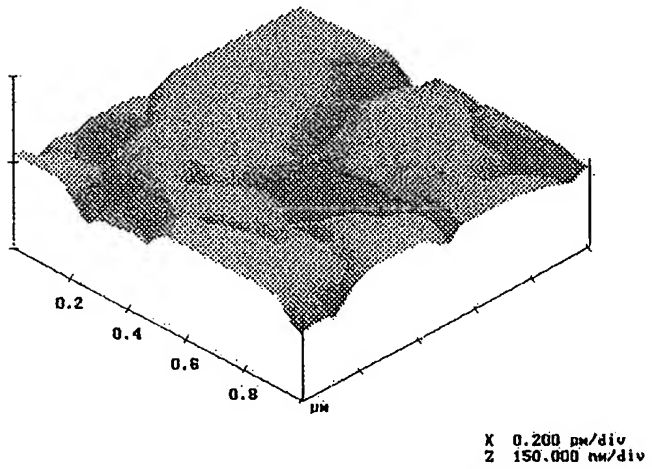

FIG. 4. AFM image of the surface of the MODFET layer in Fig. 3.

IV. CONCLUSION

The growth of high-performance AlGaN/GaN MODFETs by ammonia MBE is demonstrated. A 100-μm-wide device with a gate length of 1 μm exhibited a saturation drain current of 0.9 A/mm, a peak transconductance of 160 mS/mm, a current gain cutoff frequency of 15.6 GHz, and a maximum oscillation frequency of 49.4 GHz. The excellent dc and rf characteristics are attributed to the high mobility and high sheet charge density of the 2D electron gas in the structures grown, and to the insulating C-doped GaN buffer used in this work.

ACKNOWLEDGMENTS

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Photoluminescence characterization of p-type GaN:Mg

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ABSTRACT

We report on results of low-temperature photoluminescence measurements performed on GaN films, grown by molecular beam epitaxy (MBE) on sapphire substrates. The GaN films are either Mg doped (p-type) or consist of a Mg-doped layer on top of a Si-doped GaN layer (n-type). In the p-doped samples, the sharpness of the donor-acceptor-pair transition is striking, three phonon replicas are clearly resolved. A transition band occurs around 3.4 eV, which becomes dominant for samples with an np-layer structure. The position and the composition of the near band edge transitions are influenced by the growth of the buffer layers. Depending on the growth conditions a transition at 3.51 eV can be observed.

INTRODUCTION

The interest in GaN for application in optoelectronic devices, i.e., light-emitting diodes, has rapidly grown in recent years. The performance of the pn-junction of a diode is strongly related to the quality of the doped layers. Furthermore it has been shown [1,2] that stress, which is caused by the lattice mismatch between layers and substrate, by differences in thermal expansion coefficients and point defects, has a significant influence on the optical properties as well as on the doping properties [3]. In this respect investigations have shown that the growth of the buffer layer plays an important role in strain engineering [1,4]. The systematic control of the strain becomes more complex with increasing number of different layers.

Mg is nowadays commonly used as a p-type dopant [5] but still the properties of GaN:Mg are not fully understood. The incorporation of Mg depends also on strain and stress present in the film [3], which is determined by the buffer layer. In order to study this influence, p-type and np-type structures were grown on top of different buffer layers.

EXPERIMENTAL

The GaN samples under investigation are MBE-grown using a Riber 1000 chamber. Ga, Mg and Si are evaporated from Knudsen cells and the activated nitrogen is provided by a CGD plasma source [6]. To guarantee a homogeneous heat distribution, a thin titanium (Ti) layer is evaporated on the back of the sapphire substrates. First the substrate is nitridated at around 700 °C and then a thin GaN buffer layer with a typical thickness of 20 nm grown at 500 °C is deposited on it. Subsequently the main epitaxial GaN layer is

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grown. Typical growth conditions are: Ga source temperature 1210 K, N flow rate 5 - 80 sccm.

For this study the MBE growth process of Mg doped GaN, grown directly on the buffer layer, was optimized in order to gain high Mg incorporation and p-type mobility (sample P1 of Table 1). Furthermore a set of np-structures was produced. The thicknesses and the growth conditions of the buffer layers were varied. On the buffer layer first a Si doped GaN film (n-type) and subsequently a GaN:Mg film (p-type) was grown. The following table gives an overview of the studied samples.

Table 1: *Growth parameters of the samples under investigation.*

name	buffer layer	T(Si) [°C]	T(Mg) [°C]
P 1	6.3 nm, T=500 °C	/	280 °C
NP 1	14.6 nm, T=450 °C	1090 °C	320 °C
NP 2	7.3 nm, T=450 °C	1090 °C	320 °C
NP 3	14.6 nm, T=350 °C	1090 °C	320 °C

The thickness of the GaN:Mg layer of sample P1 is 600 nm, and the total thickness of the NP samples is 880 nm. The Mg- and Si-doped layers of the NP-samples are respectively 300 nm and 580 nm thick and they were grown in the same run.

The photoluminescence measurements were performed at low temperatures, by using a variable temperature (4 - 300 K). The samples are excited by a 50 W HeCd laser beam with a wavelength of 325 nm (3.8 eV). The spectrum of the photoluminescence light was dispersed by a double monochromator and detected by a UV photomultiplier in combination with a lock-in amplifier.

RESULTS AND DISCUSSION

Typically, the spectrum of the investigated samples can be divided into four regions. A broad emission between 2.2 and 2.5 eV, the donor-acceptor-pair (DAP) transition with its zero-phonon line (ZPL) located at 3.27 - 3.29 eV accompanied with 2 to 3 LO phonon replica, a band around 3.4 eV and several band edge related emissions between 3.45 eV and 3. 52 eV are visible.

Photoluminescence of p-type GaN

The photoluminescence of the Mg doped GaN sample (P1), which has a carrier density of $[p]=1\cdot10^{17}$ cm^{-3} and a carrier mobility of 6 cm^2/Vs is shown in Fig. 1. In the region of 2.8 - 3.3 eV the donor-acceptor-transition (DAP) has an extraordinary sharpness and the three phonon replica of the zero-phonon line (at 3.275 eV) are clearly resolved. The near band edge transitions have a relatively low intensity, as is usually expected for p-type GaN layers. The exact position of the donor bound exciton (D^0X) depends on the stress present in the layer. From the shift of the E_2 Raman mode, the energy position of the D^0X can be calculated [1] and can be used to identify this line in the photoluminescence spectrum, which is expected to be at 3.467 eV in a stress free layer at 4 K. For the sample

shown in Fig. 1, a stress of 0.71GPa was determined. Taking a stress coefficient of 27 meV / GPa into account the position of the D^0X line is calculated to be at 3.486 eV.

The photoluminescence signal of the near band edge region (Fig. 1), reaches a maximum at 3.480 eV. This transition, however, decreases strongly with increasing temperature (see Fig.1(b)) and already at 30 K a second transition at 3.486 eV becomes dominant, which can, in accordance with the Raman measurements, be identified as the D^0X transition. The other transition is located 6 meV below the D^0X and can, according to Ref.[7], be assigned to an acceptor-bound exciton (AX). At low temperatures this AX transition is even much stronger in intensity than the D^0X transition, which is consistent with the fact that this sample is p-type.

For the interpretation of the relatively weak transition, which occurs around 3.39 eV, we refer to the next section, where it is discussed in comparison to the results obtained on np-structures.

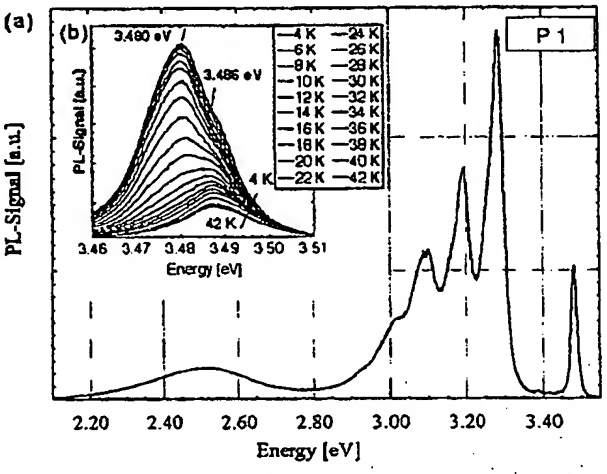

Figure 1: *The photoluminescence spectrum of a p-type MBE grown GaN:Mg sample. (a) In the spectrum a broad band in the region of 2.2 - 2.8 eV, the DAP with its 3 phonon replica (region 2.8 - 3.3 eV), and near band edge transitions are resolved. (b) The near-band edge transitions consist of the D^0X (3.486 eV) and an AX (3.480 eV) transition.*

Photoluminescence of np-structures

In this section photoluminescence spectra are studied, which have been obtained from films where a p-doped (Mg) GaN layer is deposited on top of a n-doped (Si) GaN layer grown on sapphire substrates with different buffer layers. As pointed out in Ref.[8], stress in the GaN layer doped with Si as well as the Mg doped GaN film can be modified by the growth conditions of the buffer layer. The stress in the layer has on one hand an influence on the optical properties and on the other hand the amount of incorporated dopants can be changed. In order to study this behavior three different samples with different buffer layers were grown (see Table 1).

Since the thickness of the GaN:Mg layer is 300 nm the excitation light is mainly absorbed in the p-doped layer and consequently the photoluminescence spectrum is dominated by the light emission originating from the top layer. But still it can not be

totally excluded that some emission may be due to the depletion region and the Si doped layer.

The spectra of Fig. 2 show a broad luminescence at around 2.5 eV, the donor-acceptor pair region (DAP), transitions around 3.4 eV and near-band edge transitions. In the latter two regions we observe some notable differences in the spectra, depending on the buffer layer. Certainly there is a difference in stress causing a shift of the D^0X transition. For sample NP3 an additional peak occurs at 3.51 eV, which we do not observe in other samples. The result of a temperature scan of the near band edge region is shown in Fig. 3. Two transitions, at 3.472 eV and 3.480 eV respectively, are present in the main signal, but they are so broad that they can not be resolved. A third transition at 3.51 eV however is well resolved. One possible cause for this peak could be due to the free C-exciton (FE_C) transition. In Ref.[9,10] the relation of the energy positions of A, B and C excitons is shown. According to Ref.[9] the position of the A-exciton is supposed to be located at 3.480 eV and the B-exciton at 3.488 eV. In the PL spectrum of Fig. 3 the shoulder at 3.480 eV can indeed assigned to the FE_A transition, however no FE_B transition can be resolved. The fact that there is a good agreement of the temperature dependence of the position of the A-exciton of Ref.[9] with that of the NP3 sample, as shown in the inset of Fig. 3, strengthens this assignment (cf. also Ref.[11]). The characteristic of the high-energy peak (3.51 eV) follows the slope of the A-exciton quite closely, indicating that they might be related.

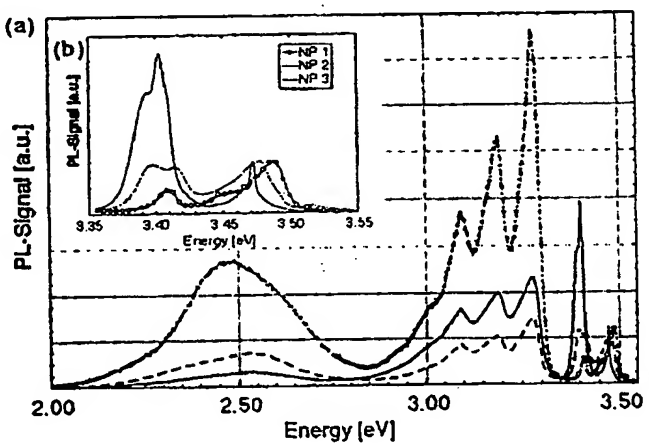

Figure 2: *Photoluminescence spectra of MBE grown samples with an np-structure (GaN:Mg layer is grown on top of a GaN:Si layer). The buffer layers were grown under different conditions (see Table 1) . (a) The spectrum consists of a broad luminescence (around 2.5 eV), the DAP with its phonon replica (region 2.8 - 3.3 eV), transitions around 3.40 eV and near band edge transitions. (b) The region above 3.35 eV is shown in more detail.*

Another explanation, that this high energy peak could originate from a transition in the depletion region, is rather unlikely, since this region should be very thin and consequently a potential emission should be very weak.

In the region of 3.38 eV -3.43 eV of Fig. 2, one to three peaks are present. The PL intensity as well as the peak positions can be modified by the growth of the buffer layer. In order to study the origin of these transitions, excitation density dependent measurements

were performed. Fig. 4 shows the result obtained on sample NP2 in logarithmic scale, and though the intensity was varied over a factor of 24 no shift in the energy position could be seen. A free-to-bound (F-B) transition, as suggested in Ref.[12], should shift towards lower energies with decreasing intensity due to band filling and a broadening of the lines would be expected [13]. None of this is observed in our measurements and in accordance to Ref. [12] we ascribe these transitions to the recombination of shallow donor- acceptor (D-A) pairs. Temperature dependent measurements show that the peak at 3.410 eV decreases strongly with increasing temperature and, at 28 K this peak is already masked by other transitions.

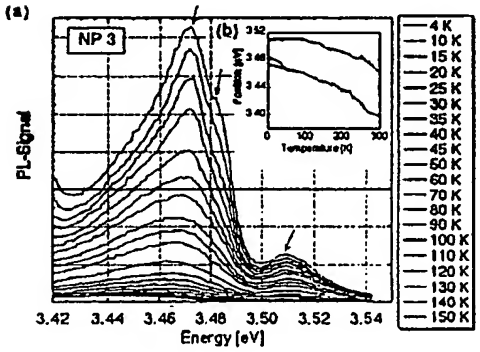

Figure 3: (a) *Temperature dependence of PL spectrum of the near-band edge transitions for sample NP3 and (b) the energy position of the peaks as function of the temperature are shown.*

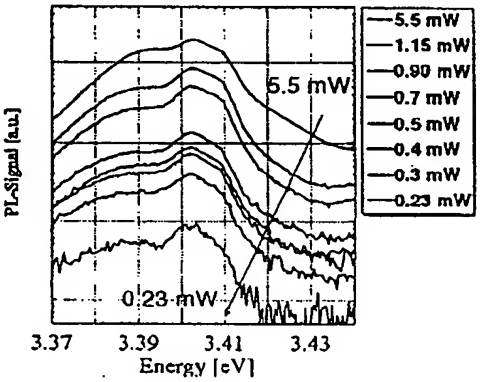

Figure 4: *The dependence of the PL spectrum on the excitation intensity of sample NP2 in the region from 3.37 eV - 3.435 is shown. The density was varied over a factor of 24.*

As mentioned earlier, the PL emission of the np samples originates mainly from the p-doped layer and therefore it is expected that the spectra of the Mg-doped sample (Fig. 1) are somehow related to those of the np-structures. Nevertheless the influence of the sub-layers on the stress, on optical properties and on the incorporation of Mg can be significant. Comparing Fig. 1 with Fig. 2 it can be seen that the spectra of sample NP1 and sample P1 are in good agreement. Both exhibit very well resolved phonon replicas of the DAP transition and the ratio of the near band edge PL signal to the DAP signal is very low, typical for p-doping.

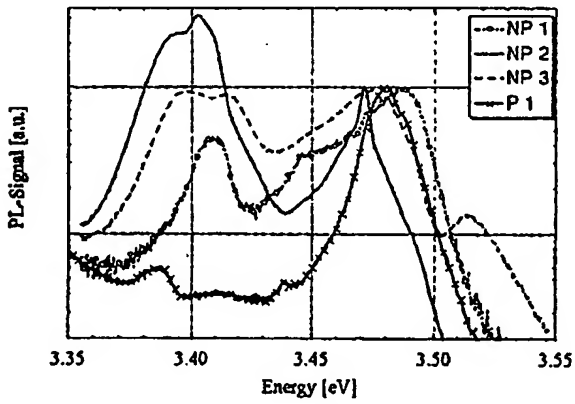

Figure 5: *The PL spectrum (in logarithmic scale) in the region from 3.35 eV to 3.55 eV of the p-type sample (P1) is shown in comparison to the np-structures.*

The region above 3.35 eV is of special concern and therefore the spectra are shown in Fig. 5 in more detail. Striking is the fact that, even in sample P1, there is a transition in the region of 3.4 eV (at 3.385 eV), but it is very weak compared to the signal of the np-structures. Depending on the buffer layer growth the intensity changes and this transition even becomes dominant for sample NP2.

SUMMARY

Photoluminescence signals of MBE grown samples consisting of a Mg-doped GaN (p-type) layer on top of a Si-doped GaN (n-type) layer were compared to the spectrum of a GaN:Mg layer grown directly on a GaN buffer layer. The DAP transition in the 2.80 - 3.38 eV region and its phonon replica are very well resolved and typically dominate the spectra. In the region of 3.38 eV - 3.43 eV shallow donor-acceptor pair recombination transitions are observed, which become significant in intensity for np-structures. Depending on the growth conditions of the buffer layer an additional transition at 3.51 eV is observed. Based on temperature-dependent measurements we suggest that this line is due to a FE_C exciton.

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DERWENT-ACC-NO: 2002-198483

DERWENT-WEEK: 200226

TITLE: Low resistant gallium nitride group buffer layer for field effect transistor, metal semiconductor field effect transistor, comprises multiple thin layers of nitride group compound semiconductor containing gallium

PATENT-ASSIGNEE: FURUKAWA ELECTRIC CO LTD[FURU]

PRIORITY-DATA: 2000JP-0084613 (March 24, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
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APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
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INT-CL (IPC): C30B029/38, H01L021/203 , H01L021/338 , H01L029/778 , H01L029/812 , H01L033/00 , H01S005/32

ABSTRACTED-PUB-NO: JP2001274376A

BASIC-ABSTRACT:

NOVELTY - A low resistant gallium nitride group buffer layer (2) comprises
multiple thin layers (2A-2C) of nitride group III-V group compound
semiconductor containing gallium as essential component.

USE - For field effect transistor, metal semiconductor field effect transistor.

ADVANTAGE - GaN group buffer layer of low resistance is offered. High
industrial usage is offered. The two dimensional electron gas layer formed on
heterojunction boundary surface of compound semiconductor of high purity, is
utilized effectively.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of buffer layer
structure.

Buffer layer 2

Thin layers 2A-2C

CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: LOW RESISTANCE GALLIUM NITRIDE GROUP BUFFER LAYER FIELD EFFECT
TRANSISTOR METAL SEMICONDUCTOR FIELD EFFECT TRANSISTOR COMPRISE

MULTIPLE THIN LAYER NITRIDE GROUP COMPOUND SEMICONDUCTOR CONTAIN GALLIUM

DERWENT-CLASS: L03 U11 U12 V08

CPI-CODES: L04-A02A1A; L04-E01A;

EPI-CODES: U11-C01A1; U11-C18A3; U12-D02B; U12-D02D2; V08-A04A;

SECONDARY-ACC-NO:
CPI Secondary Accession Numbers: C2002-061344
Non-CPI Secondary Accession Numbers: N2002-150970

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	21/338		H01L	21/203	M	5F041
	29/812			33/00	C	5F073
C30B	29/38		H01S	5/32		5F102
H01L	21/203		H01L	29/80	H	5F103

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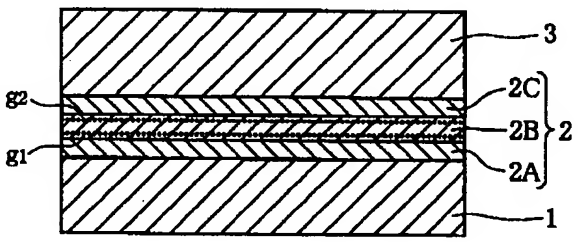
(54)【発明の名称】　低抵抗ＧａＮ系緩衝層

(57)【要約】
【課題】　低抵抗のＧａＮ系緩衝層を提供する。
【解決手段】　この緩衝層２は、Ｇａを必須成分として含む窒化物系III－Ｖ族化合物半導体から成る少なくとも２層の薄層をヘテロ接合した層構造、例えばＡｌＧａＮ 2Ａ／ＧａＮ 2Ｂ／ＡｌＧａＮ 2Ｃになっていて、このヘテロ結合界面に形成される２次元電子ガス層を積極的に活用しているので低抵抗になっている。



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【特許請求の範囲】

【請求項1】　Gaを必須成分として含む窒化物系III－V族化合物半導体から成る少なくとも2層の薄層をヘテロ接合した層構造になっていることを特徴とする低抵抗GaN系緩衝層。

【請求項2】　前記層構造が、AlGaN／GaN／AlGaN，GaN／AlGaN／GaN，GaN／InGaN／GaN，InGaN／GaN／InGaN，InAlGaN／GaN／InAlGaN（ただし、InAlGaNは、GaNよりもバンドギャップエネルギーが大きい組成になっている），GaN／InAlGaN／GaN，AlGaNP／GaNP／AlGaNP，AlGaNAs／GaNAs／AlGaNAs，AlGaNP／InGaNP／AlGaNP，AlGaNAs／InGaNAs／AlGaNAsのいずれかである請求項1の低抵抗GaN系緩衝層。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は基板の上にエピタキシャル成長法で成膜される低抵抗GaN系緩衝層に関し、更に詳しくは、FETやMESFETのような各種のGaN系半導体素子の製造時に採用することにより、当該半導体素子の基板裏面への動作電極の形成を可能にした低抵抗GaN系緩衝層に関する。

【0002】

【従来の技術】例えばGaN系材料でFETを製造する場合には、基板の上に例えばMOCVD法やMBE法のようなエピタキシャル成長法で所定の組成を有するGaN系結晶層を順次積層してFET層構造を形成することが必要である。その場合、GaN系材料と格子定数が一致する基板材料は皆無であるため、異種材料から成る基板が結晶成長用の基板として用いられている。通常はサファイア基板が用いられている。

【0003】しかしながら、このサファイア基板と結晶成長するGaN結晶との格子不整合率は20%以上であるため、両者の格子不整合を緩和し、成膜されたGaN結晶における結晶欠陥を極力少なくすることを目的として、サファイア基板の上には、一旦、緩衝層を成膜することが行われている。通常、この緩衝層はノンドープの状態で成膜され、そしてその上に所望する膜厚のn型GaN結晶層をn型活性層として成膜することによりGaN系のFET層構造が形成されることになる。

【0004】上記した緩衝層の成膜に関しては、従来から次のような2段階成長法が適用されている。第1の方法は、通常、MOCVD法により、例えばトリエチルアルミニウム（TEA）とアンモニア（NH_3）を用い、水素をキャリアガスとして用い、成長温度800℃でサファイア基板上に、一旦、厚み5nm程度の極薄なAlN層を下部緩衝層として成膜し、ついで成長温度を1100℃に上昇させ、トリメチルガリウム（TMG）とアンモニア（NH_3）を用いて厚膜のノンドープGaN結晶層を上部緩衝層として前記AlN層の上に成膜する方法である。

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【0005】また、第2の方法としては次のような方法が適用されている。すなわち、MOCVD法により、例えばTMGとNH_3を用い、水素をキャリアガスとして用い、温度500～600℃の低温下で厚み1～2nm程度の非晶質GaN層を下部緩衝層として成膜し、ついで温度を1100℃に上昇してエピタキシャル成長を行い、前記非晶質GaN層の上に厚膜のノンドープGaN結晶層を上部緩衝層として成膜する方法である。

【0006】このようにして成膜された従来のGaN系緩衝層は、結晶欠陥が多いという問題と、同時に、上部緩衝層として成膜されている厚膜のノンドープGaN結晶層が高抵抗であるということに規定されて緩衝層全体としては高抵抗になっているという問題を有している。

【0007】

【発明が解決しようとする課題】ところで、例えば縦型のGaN系FETを製造しようとする場合には、基板として導電性材料から成る基板を用い、製造した素子の上面と、下面（すなわち基板裏面）にそれぞれ動作電極を形成することが必要になる。しかしながら、上記の従来方法で形成したFET構造においては、基板上に位置する緩衝層が高抵抗になっているため、基板の裏面に動作電極を形成しても電極動作を示さないことになる。したがって、縦型のGaN系FETを製造しようとする場合には、緩衝層をノンドープの状態で、かつ低抵抗にすることが必要になる。

【0008】本発明は、上記した要請に応えることができ、高純度であると同時に、低抵抗であるGaN系緩衝層の提供を目的とする。

【0009】

【課題を解決するための手段】本発明者は上記した目的を達成するために研究を重ねる過程で、HEMTの場合に代表されるように、互いに高純度である化合物半導体のヘテロ接合界面には2次元電子ガス層が形成され、その領域における電子は高い移動度を有するという事実に着目した。そして、上記したGaN系の緩衝層の場合でも、複数の高純度なGaN系材料を用いてヘテロ接合構造を形成すれば、互いのヘテロ接合界面には2次元電子ガス層が形成され、そのことにより、緩衝層を全体として低抵抗化することが可能になるとの着想を抱き、その着想に基づいて更に研究を重ねた結果、上記着想が正当であることを確認し、本発明を開発するに至った。

【0010】すなわち、本発明の低抵抗GaN緩衝層は、Gaを必須成分として含む窒化物系III－V族化合物半導体から成る少なくとも2層の薄層をヘテロ接合した層構造になっていることを特徴とする。そして、このような層構造としては、AlGaN／GaN／AlGaN，GaN／AlGaN／GaN，GaN／InGaN

／GaN，InGaN／GaN／InGaN，InAlGaN／GaN／InAlGaN（ただし、InAlGaNは、GaNよりもバンドギャップエネルギーが大きい組成になっている），GaN／InAlGaN／GaN，AlGaNP／GaNP／AlGaNP，AlGaNAs／GaNAs／AlGaNAs，AlGaNP／InGaNP／AlGaNP，AlGaNAs／InGaNAs／AlGaNAsのいずれかであることを好適とする。

【0011】

【発明の実施の形態】以下、図面に基づいて本発明の緩衝層を説明する。図1は、基板1の上に、後述する高純度な緩衝層2が成膜され、更にその上に、SiドープGaN結晶層のような同じく高純度な緩衝層2が成膜され、更にその上に、SiドープGaN結晶層のような同じく高純度なn型活性層3が形成された断面構造を示す。

【0012】ここで、基板1としては、例えばSi，SiC，GaAs，GaP，InPなどの基板のヘテロ接合から成る層構造のような導電性材料から成る基板を用いれば、この材料からは、n型活性層3に上部電極を、基板1の裏面に下部電極をそれぞれ形成することにより、縦型のFETを製造することができる。緩衝層2は、全体として、第1緩衝層2A、第2緩衝層2B、および第3緩衝層2Cから成る3層構造になっていて、各部分緩衝層の接合界面はヘテロ接合界面になっている。

【0013】そして、これら緩衝層2A，2B，2Cは、Gaを必須成分として含む窒化物系III－V族化合物半導体で構成されていて、図1の材料の場合、具体的には、第1緩衝層2AはAlGaN（Al：15原子%）結晶層、第2緩衝層2BはGaN結晶層、第3緩衝層2CはAlGaN（Al：20原子%）結晶層になっている。

【0014】この緩衝層2の場合、第1緩衝層2Aと第2緩衝層2Bの接合界面における第2緩衝層2B側には2次元電子ガス層g_1が形成され、また、第2緩衝層2Bと第3緩衝層2Cの接合界面における第2緩衝層2B側にも2次元電子ガス層g_2が形成されることになる。すなわち、2つの接合界面に対応して第2緩衝層2Bの上下には2つの2次元電子ガス層が形成されている。

【0015】したがって、この第2緩衝層2Bを薄く成膜することにより、上記した2次元電子ガス層g_1，g_2の作用で、当該第2緩衝層2Bの上下方向における抵抗を低めることが可能になる。具体的には、第2緩衝層2Bの厚みを10nm以下に設定すれば、上下方向における導電性を発現せしめることができる。なお、第1緩衝層2Aと第3緩衝層2Cは、いずれも、第2緩衝層2Bとの接合界面に2次元電子ガス層を形成するためにのみ成膜されるものである。したがって、その材料としては、第2緩衝層2Bにおける材料のバンドギャップエネルギーよりも大きいバンドギャップエネルギーを有する組成のものが選定される。そして、これら層2A，2Cの厚みは厚くなくてよく、上記した2次元電子ガス層の形成に必要な厚みであれば充分である。むしろ、層2A，2Cの厚みを厚くすると、緩衝層全体の上下方向における抵抗を高めるようになる。したがって、成膜時に層2A，2Cを平坦面にするということも勘案して30～50nm程度に設定すればよい。

【0016】このような作用効果を発揮する緩衝層2の層構造としては、それを、第1緩衝層2A／第2緩衝層2B／第3緩衝層3Cで表現した場合、次のような層構造を好適例としてあげることができる。すなわち、AlGaN／GaN／AlGaN，GaN／AlGaN／GaN，GaN／InGaN／GaN，InGaN／GaN／InGaN，InAlGaN／GaN／InAlGaN（ただし、InAlGaNは、GaNよりもバンドギャップエネルギーが大きい組成になっている），GaN／InAlGaN／GaN，AlGaNP／GaNP／AlGaNP，AlGaNAs／GaNAs／AlGaNAs，AlGaNP／InGaNP／AlGaNP，AlGaNAs／InGaNAs／AlGaNAsのいずれかである。

【0017】

【実施例】実施例1

図1で示した材料をMBE法で次のようにして製造した。導電性のSi基板1の上に、成長温度750℃で、まず、1原子層のAlを堆積させた。

【0018】ついで、プラズマ化した窒素（3×10^{-6}Torr）、金属Ga（5×10^{-7}Torr）、金属Al（1×10^{-7}Torr）、および金属Si（1×10^{-9}Torr）を用い、成長温度800℃で厚み3nmのSi添加AlGaN（Al：15原子%）結晶層を第1緩衝層2Aとして成膜した。この層の表面のストリークパターンを高速電子線回折装置（RHEED）で観察したところ平坦であることが確認された。

【0019】ついで、プラズマ化した窒素（3×10^{-6}Torr）、金属Ga（5×10^{-7}Torr）のみを用いて上記第1緩衝層2Aの上に厚み30nmのGaN結晶層を第2緩衝層2Bとして成膜した。RHEED観察によればこの層の表面も平坦であった。更に、上記ガス源に金属Al（2×10^{-7}Torr）を加えてMBE法を行い、上記第2緩衝層2Bの上に厚み3nmのAlGaN（Al：20原子%）結晶層を第3緩衝層2Cとして成膜した。RHEED観察によればこの層の表面も平坦であった。

【0020】ついで、プラズマ化した窒素（5×10^{-5}Torr）と金属Ga（8×10^{-7}Torr）を用い、n型ドーパントとして金属Si（5×10^{-8}Torr）を用い、成長温度850℃で上記第3緩衝層2Cの上に厚み30nmのSiドープGaN結晶層をn型活性層3として成膜した。得られた材料につき、C－V測定を行って、緩衝層

のあるヘテロ接合付近のキャリア濃度を調べたところ、緩衝層2とn型活性層3との界面におけるキャリア濃度は$3\times10^{18}cm^{-3}$であり、充分に上下方向の導電性を有することが確認された。このことは、緩衝層に2次元電子ガス層が形成されていることを根拠づけるものである。

【0021】実施例2

MBE法により、導電性のSi基板1の上に成長温度700℃で、まず、1原子層のGaを堆積させた。ついで、プラズマ化した窒素（3×10^{-6}Torr）、金属Ga（5×10^{-7}Torr）、および金属Si（1×10^{-9}Torr）を用い、成長温度800℃で厚み3nmのSi添加GaN結晶層を第1緩衝層2Aとして成膜した。この層の表面のストリークパターンを高速電子線回折装置（RHEED）で観察したところ平坦であることが確認された。

【0022】ついで、プラズマ化した窒素（3×10^{-6}Torr）、金属Ga（8×10^{-7}Torr）および金属Al（1×10^{-7}Torr）を用いて上記第1緩衝層2Aの上に厚み30nmのAlGaN（Al：15原子%）結晶層を第2緩衝層2Bとして成膜した。RHEED観察によればこの層の表面も平坦であった。ついで、金属Alの供給を絶ってMBE法を行い、上記第2緩衝層2Bの上に厚み3nmのGaN結晶層を第3緩衝層2Cとして成膜した。RHEED観察によればこの層の表面も平坦であった。

【0023】そして、プラズマ化した窒素（5×10^{-5}Torr）と金属Ga（8×10^{-7}Torr）を用い、n型ドーパントとして金属Si（5×10^{-8}Torr）を用い、成長温度850℃で上記第3緩衝層2Cの上に厚み300nmのSiドープGaN結晶層をn型活性層3として成膜した。得られた材料につき、C－V測定を行って、緩衝層付近のキャリア濃度を調べたところ、緩衝層2とn型活性層3との界面におけるキャリア濃度は$5\times10^{18}cm^{-3}$であり、充分に上下方向の導電性を有することが確認された。

【0024】なお、上記実施例において、GaN結晶層の成膜用窒素源としてはラジカル化した窒素やアンモニアを用いてもよく、Ga源としてはトリメチルガリウム（TMG）やトリエチルガリウム（TEG）などの有機金属ガスを用い、Al源としてはトリメチルアルミニウム（TMA）やトリエチルアルミニウム（TEA）などの有機金属ガスを用いてもよく、また、不純物としてはSiに代えてシランガスを用いてもよい。

【0025】更に、上記実施例では、エピタキシャル成長法としてMBE法を採用したが、上記した有機金属ガスを用いたMOCVD法を適用しても同様の結果をえることができる。

【0026】

【発明の効果】以上の説明で明らかなように、本発明の低抵抗GaN系緩衝層は、高純度の化合物半導体のヘテロ接合界面に形成される2次元電子ガス層を積極的に活用したものである。したがって、この緩衝層を用いることにより、縦型のGaN系FETやGaN系MESFETの製造が可能となり、その工業的価値は大である。

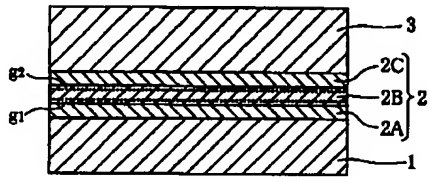
【図面の簡単な説明】

【図1】本発明の緩衝層を用いた層構造を示す断面図である。

【符号の説明】

1	結晶成長用の基板（導電性Si基板）
2	緩衝層
2A	第1緩衝層（AlGaN）
2B	第2緩衝層（GaN）
2C	第3緩衝層（AlGaN）
3	n型活性層（SiドープGaN）

【図1】



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HA06
5F041 AA40 CA34 CA40
5F073 CA07 CA17 CB04 CB07 DA05
DA06
5F102 GB01 GC01 GD01 GJ03 GJ04
GJ05 GJ06 GK08 GQ01 HC01
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(71)Applicant : SANKEN ELECTRIC CO LTD

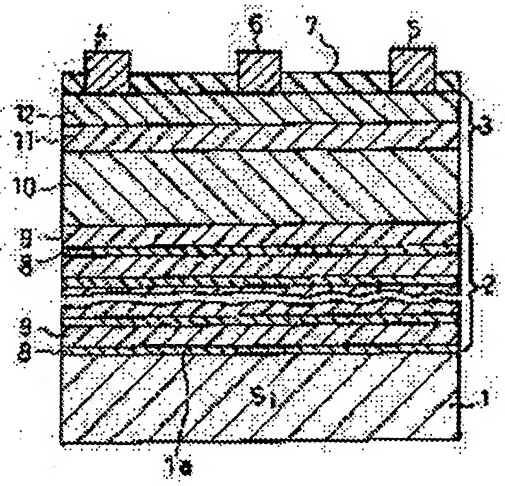
(72)Inventor : MOKU TETSUJI
OTSUKA KOJI

(54) SEMICONDUCTOR DEVICE AND PRODUCTION METHOD THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the costs of a GaN compound semiconductor device.

SOLUTION: A buffer layer 2 is provided with the structure of alternately laminating a plurality of first layers 8 composed of Al and second layers 9 composed of GaN on a wafer 1 composed of silicon. A gallium-nitride semiconductor region 3 for HEMT element is formed on the buffer layer 2.



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[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
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3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The substrate which is the semiconductor device which has a nitride system compound semiconductor, and consists of silicon or a silicon compound, The semiconductor region for semiconductor devices containing at least one nitride system compound semiconductor layer which has been arranged on one principal plane of said substrate, and has been arranged on a buffer layer and said buffer layer, the 1st main electrode, 2nd main electrode, and control electrode which have been arranged on the front face of said semiconductor region for semiconductor devices -- having -- said buffer layer -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which it is here and said

前記x及びyは、 $0<x\leqq1$、
$0\leqq y<1$、
$x+y\leqq1$

M was chosen from In (indium) and B (boron),

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula AlaMbGa1-a-bN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

前記a及びbは、 $0\leqq a\leqq1$、
$0\leqq b<1$、
$a+b\leqq1$

the numeric value to satisfy and the semiconductor device which comes out and is characterized by consisting of a compound layer with the 2nd layer which consists of the ingredient shown.
[Claim 2] It is the semiconductor device according to claim 1 characterized by for said 1st layer consisting of AlxGa1-xN, and said 2nd layer consisting of AlaGa1-aN.
[Claim 3] It is the semiconductor device according to claim 1 characterized by for said 1st layer consisting of AlxInyGa1-x-yN, and for said 2nd layer consisting of AlaInbGa1-a-bN, and containing In (indium) at least in one side of said 1st and 2nd layers.
[Claim 4] It is the semiconductor device according to claim 1 characterized by for said 1st layer consisting of AlxByGa1-x-yN, and for said 2nd layer consisting of AlaBbGa1-a-bN, and containing B (boron) at least in one side of said 1st and 2nd layers.
[Claim 5] Said buffer layer is a semiconductor device according to claim 1, 2, 3, or 4 characterized by consisting of said two or more 1st and 2nd layers, and carrying out the laminating of said the 1st layer and said 2nd layer by turns.
[Claim 6] A semiconductor device claim 1 to which thickness of said 1st layer in said buffer layer is characterized by the thickness of 0.5nm - 50nm and said 2nd layer being 0.5nm - 200nm, 2, or given in three.
[Claim 7] The principal plane of the side by which said buffer layer of said substrate is arranged is a semiconductor device according to claim 1 characterized by being the field to which it leans in -4 to +4 times from the field or (111) the field just (111) in field bearing of the crystal shown with Miller indices.
[Claim 8] Said nitride system compound semiconductor layer is a semiconductor device according to claim 1 characterized by being chosen from a GaN (gallium nitride) layer, an AlInN (indium nitride aluminum) layer, an AlGaN (gallium nitride aluminum) layer, an InGaN (gallium nitride indium) layer, and an AlInGaN (gallium nitride indium aluminum) layer.

[Claim 9] It is the semiconductor device according to claim 1 which said semiconductor region consists of two or more semi-conductor layers for forming a field-effect transistor, said 1st main electrode is a source electrode, and said 2nd main electrode is a drain electrode, and is characterized by said control electrode being a gate electrode.
[Claim 10] Said semiconductor region is a semiconductor device according to claim 1 characterized by consisting of two or more semi-conductor layers for forming a high electron mobility transistor (HEMT).
[Claim 11] Said semiconductor region is a semiconductor device according to claim 1 characterized by consisting of two or more semi-conductor layers for forming a metal semiconductor field-effect transistor (MESFET).
[Claim 12] the process which prepares the substrate which is the manufacture approach of a semiconductor device of having a nitride system compound semiconductor, and consists of silicon or a silicon compound, and said substrate top -- vapor growth -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula At least one sort of elements with which said M was chosen from In (indium) and B (boron) AlaMbGa1-a-bN and here,

前記a及びbは、 $0<a\leqq 1$、
$0\leqq b<1$、
$a+b\leqq 1$

the manufacture approach of the semiconductor device characterized by to have the process which forms the numeric value to satisfy and the 2nd layer which comes out and consists of the ingredient shown one by one, and obtains a buffer layer, the process which form the semiconductor region for semiconductor devices which consists of at least one nitride system compound semiconductor layer by vapor growth on said buffer layer, and the process which form the 1st and 2nd main electrodes and control electrodes on the front face of said semiconductor region for semiconductor devices.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a semiconductor device and its manufacture approaches, such as MESFET which used the nitride system compound semiconductor, and HEMT.
[0002]
[Description of the Prior Art] Semiconductor devices, the metal semiconductor field-effect transistor (High Electron Mobility Transistor), i.e., MESFET (Metal Semiconductor Filed Effect Transistor) and a high electron mobility transistor, i.e., HEMT etc., using a gallium nitride system compound semiconductor etc., are well-known. in the semiconductor device using the conventional typical gallium nitride system compound semiconductor, it consists of about 500-600-degree C GaN or AlN comparatively formed at low-temperature substrate temperature on the insulating substrate which consists of sapphire -- it minds a low-temperature buffer layer (only henceforth a low-temperature buffer layer), and a compound semiconductor is formed.
[0003] That is, in forming MESFET, it forms on the insulating substrate which consists of sapphire, the layer of operation, i.e., the channel layer, which consists of the n form GaN layer which doped Si through the low-temperature buffer layer which consists of GaN or AlN, and forms a source electrode, a drain electrode, and a gate electrode in the front face of a layer of operation. Moreover, in forming HEMT, on the insulating substrate which consists of sapphire, the laminating of the electronic supply layer, the electronic transit layer, i.e., the channel layer, which consists of non-doping GaN through the low-temperature buffer layer which consists of GaN or AlN, which consists of the n form AlGaN is carried out, it is formed, and it forms a source electrode, a drain electrode, and a gate electrode in the front face of an electronic supply layer.
[0004]
[Problem(s) to be Solved by the Invention] By the way, this kind of a gallium nitride system or a nitride system semiconductor device cuts down the wafer which many components made as everyone knows and was full according to dicing, scribing, a cleavage (cleavage), etc., and is formed. Since the insulating substrate which consists of sapphire at this time had the high degree of hardness, it was difficult to perform this dicing etc. with sufficient productivity. Moreover, since sapphire was expensive, the cost of a semiconductor device became high. Moreover, when carrying out crystal growth of the nitride system compound semiconductor on silicon on sapphire, in order to obtain a flat nitride system compound semiconductor layer, it is necessary to form a low-temperature buffer layer as mentioned above. If crystal growth of the nitride system compound semiconductor layer is carried out at an elevated temperature through a low-temperature buffer layer, the comparatively flat nitride system compound semiconductor film can be formed on silicon on sapphire. However, at low temperature, when the low-temperature buffer layer which consists of GaN or AlN is formed, since the ammonia used as a nitrogen source hardly disassembles, a low-temperature buffer layer becomes an amorphous layer containing metal-like Ga and aluminum. Since crystal growth of a channel layer, i.e., the layer of operation etc., is carried out on the buffer layer of this amorphous condition, in the field near a low-temperature buffer layer, the consistency of a crystal defect becomes very high. Since the high field of this defect density functions as an n type semiconductor layer of low resistance, when operating a device, a current leaks it also to this n type semiconductor layer in addition to a layer (channel layer) of operation. Consequently, a good pinch-off property is no longer acquired. As an approach of solving this problem, [redacted] buffer layer and a channel layer, and the technique of controlling current leak in a low resistance [redacted]

layer is proposed by JP,2000-299325,A. However, in order that mediation of an AlGaN layer may generate distortion which originated in the epitaxial layer at the stacking fault, it reduces the electron mobility of a channel layer and invites the problem of making a channel layer generate a crack further etc. For this reason, it was difficult to restrain A1 amount and thickness of an AlGaN layer and to fully control leakage current as a result.

[0005] Moreover, the heat conductivity of silicon on sapphire could not fully emit the heat generated working [a device] since it is small, 0.126 W/cm-K and, but caused the fall of many properties of a transistor, such as reducing pressure-proofing, gain, etc. of a device. Furthermore, although the hetero structure which carried out the laminating of the AlGaN is generally adopted on the GaN layer by the GaN system HEMT, when growing up AlGaN on a GaN layer, a stacking fault pulls to the field inboard in AlGaN, and distortion is generated. For this stress, piezo polarization electric field occur in an interface, and if it combines with spontaneous polarization, the electric field of several MV/cm will occur in a hetero interface. Into a channel, it is accumulated by this electric field, the two-dimensional electron gas EG, i.e., 2D, of 1013cm-2 order, the fall of channel sheet resistance is achieved, and a drain current can be made to increase. This is the advantage of the GaN system HEMT which adopted the hetero structure which carried out the laminating of the AlGaN on the GaN layer.

[0006] however, silicon on sapphire -- since a coefficient of thermal expansion is larger than a nitride system compound semiconductor -- heat -- therefore, an epitaxial layer is made to generate a compressive strain irregularly Since this compressive strain works in the direction which cancels the hauling distortion in AlGaN resulting from a stacking fault, it will decrease piezo polarization electric field. For this reason, the concentration of electrons of 2D EG also falls and the engine performance of the AlGaN/GaN system HEMT cannot fully be demonstrated.

[0007] Then, the purpose of this invention is to offer a semiconductor device and its manufacture approaches, such as MESFET using the nitride system compound semiconductor which can solve an above-mentioned trouble, and HEMT.

[0008]

[Means for Solving the Problem] This invention for solving the above-mentioned technical problem and attaining the above-mentioned purpose The substrate which is the semiconductor device which has a nitride system compound semiconductor, and consists of silicon or a silicon compound, The semiconductor region for semiconductor devices containing at least one nitride system compound semiconductor layer which has been arranged on one principal plane of said substrate, and has been arranged on a buffer layer and said buffer layer, the 1st main electrode, 2nd main electrode, and control electrode which have been arranged on the front face of said semiconductor region for semiconductor devices -- having -- said buffer layer -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which it is here and said M was chosen from In (indium) and B (boron),

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula AlaMbGa1-a-bN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

前記a及びbは、 $0\leqq a\leqq 1$、
$0\leqq b<1$、
$a+b\leqq 1$

the numeric value to satisfy and the semiconductor device characterized by consisting of a compound layer with the 2nd layer which comes out and consists of the ingredient shown are started.

[0009] In addition, as shown in claim 2, said 1st layer can be set to AlxGa1-xN, and said 2nd layer can be set to AlaGa1-aN. Moreover, as shown in claim 3, said 1st layer can be made into AlxInyGa1-x-yN, said 2nd layer can be made into AlaInbGa1-a-bN, and In (indium) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 4, said 1st layer can be made into AlxByGa1-x-yN, said 2nd layer can be made into AlaBbGa1-a-bN, and B (boron) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 5, as for said buffer layer, it is desirable to consist of said two or more 1st and 2nd layers, and to carry out the laminating of said the 1st layer and said 2nd layer by turns. Moreover, as shown in claim 6, it is desirable for the thickness of said 1st layer in said buffer layer to be [for the thickness of 0.5nm - 50nm and said 2nd layer] 0.5nm - 200nm. As shown in

claim 7, as for the principal plane of the side by which said buffer layer of said substrate is arranged, it is desirable that it is the field to which it leans in -4 to +4 times from the field or (111) the field just (111) in field bearing of the crystal shown with Miller indices. Moreover, as shown in claim 8, as for said nitride system compound semiconductor layer, it is desirable to be chosen from a GaN (gallium nitride) layer, an AlInN (indium nitride aluminum) layer, an AlGaN (gallium nitride aluminum) layer, an InGaN (gallium nitride indium) layer, and an AlInGaN (gallium nitride indium aluminum) layer. Moreover, as shown in claim 9, said semiconductor region can be used as two or more semi-conductor layers for forming a field-effect transistor, said 1st main electrode can be used as a source electrode, said 2nd main electrode can be used as a drain electrode, and said control electrode can be used as a gate electrode. Moreover, as shown in claim 10, said semiconductor region can be used as two or more semi-conductor layers for forming a high electron mobility transistor (HEMT). Moreover, as shown in claim 11, said semiconductor region can be used as two or more semi-conductor layers for forming a metal semiconductor field-effect transistor (MESFET). moreover, the process which prepares the substrate which consists of silicon or a silicon compound in the manufacture approach of a semiconductor device of having a nitride system compound semiconductor as shown in claim 12 and said substrate top -- vapor growth -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula At least one sort of elements with which said M was chosen from In (indium) and B (boron) AlaMbGa1-a-bN and here,

前記a及びbは、 $0<a\leqq 1$、
$0\leqq b<1$、
$a+b\leqq 1$

it is desirable to have the process which forms the numeric value to satisfy and the 2nd layer which comes out and consists of the ingredient shown one by one, and obtains a buffer layer, the process which forms the semiconductor region for semiconductor devices which consists of at least one nitride system compound semiconductor layer by vapor growth on said buffer layer, and the process which forms the 1st and 2nd main electrodes and control electrodes on the front face of said semiconductor region for semiconductor devices.

[0010]

[Effect of the Invention] According to invention of each claim, the following effectiveness is acquired.

(1) Since the substrate with which it is low cost and workability also consists of good silicon or a good silicon compound is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of a semiconductor device is possible.

(2) The buffer layer to which the lattice constant formed in one principal plane of a substrate changes from the 1st layer 8 which has a value between silicon and GaN, and the 2nd layer can succeed the crystal orientation of a substrate good. Consequently, crystal orientation can be arranged and a nitride system semiconductor region can be formed in one principal plane of a buffer layer good. For this reason, the surface smoothness of a semiconductor region becomes good and the electrical characteristics of a semiconductor device also become good. When a buffer layer is formed in one principal plane of the substrate which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the nitride system semiconductor region excellent in surface smoothness in the top face of this buffer layer.

(3) As compared with the low temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer which consists of the compound layer of the 1st layer 8 and the 2nd layer 9 can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase, i.e., a semiconductor region, formed on a buffer layer can be made small enough, and generating of leakage current can be prevented.

(4) Since a substrate is formed from the silicon or the silicon compound which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate,

and many properties, such as pressure-proofing of a device and gain, are acquired good. The indium is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 3. The stress relaxation effectiveness between the nitride system compound semiconductor (indium nitride system compound semiconductor) containing an indium, then a substrate and a nitride system semiconductor region is acquired still better at least in one side of the 1st and 2nd layers. That is, as compared with other nitride system compound semiconductors which do not contain In as a configuration element, for example, GaN, AlN, etc., the substrate and coefficient of thermal expansion which consist of silicon or a silicon compound approximate more the indium nitride system compound semiconductor which constitutes at least one side of the 1st and 2nd layers, for example, InN, InGaN, AlInN, AlInGaN, etc. For this reason, distortion of the semiconductor region resulting from the difference of the coefficient of thermal expansion between a substrate and a nitride system semiconductor region can be prevented good by including an indium in one [at least] layer among the 1st layer and the 2nd layer which constitute a buffer layer. B (boron) is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 4. The buffer layer containing B (boron) has a coefficient of thermal expansion near the coefficient of thermal expansion of the substrate which consists of silicon or a silicon compound rather than the buffer layer which does not have B (boron) **. For this reason, according to the buffer layer containing B (boron), distortion of the nitride system semiconductor region resulting from the coefficient-of-thermal-expansion difference between the substrates and nitride system semiconductor regions which consist of silicon or a silicon compound can be prevented good. In invention of claim 5, since the laminating of two or more 1st layers and two or more 2nd layers is carried out by turns and a buffer layer is constituted, two or more 1st thin layers are distributed. Consequently, buffer ability good as the whole buffer layer can be obtained, and the crystallinity of the semiconductor region formed on a buffer layer becomes good. According to invention of claim 6, the buffer ability of a buffer layer can improve and surface smoothness of a nitride system semiconductor region can be improved. According to invention of claim 7, a buffer layer and a semiconductor region can be formed good on a substrate. namely, the thing abolished for the atomic step on the front face of a crystal of a buffer layer and a semiconductor region, i.e., the step in atomic level, by making field bearing of the principal plane of a substrate into a field or (111) the field from a field where an OFF include angle is small just (111) -- or it can lessen. If a buffer layer and a semiconductor region are formed on a principal plane with the large off include angle from a field just (111), it will see on atomic level to this etc., and a comparatively large step will arise. Although some steps do not become a problem so much when an epitaxial growth phase is comparatively thick, in the case of the semiconductor device which has the film of thickness, there is a possibility of causing the fall of a property. On the other hand, a field or the field where an off include angle is small, then a step become small just (111) about the principal plane of a substrate, and a buffer layer and a semiconductor region are formed good. According to invention of claim 12, a semiconductor device with a sufficient property can be formed cheaply and easily.

[0011]

[The 1st operation gestalt] Next, HEMT using the gallium nitride system compound semiconductor applied to the 1st operation gestalt of this invention with reference to drawing 1 - drawing 3 is explained.

[0012] HEMT concerning the 1st operation gestalt of this invention shown in drawing 1 consists of a buffer layer, the substrate 1, i.e., the substrate, which consists of silicon, 2, the semiconductor region 3 for HEMT elements, the source electrode 4 as the 1st electrode, the drain electrode 5 as the 2nd electrode, the gate electrode 6 as a control electrode, and an insulator layer 7.

[0013] The HEMT element semiconductor region 3 has the electronic transit layer 10 which consists of impurity non-doping GaN, the spacer layer 11 which consists of non-doping aluminum0.2Ga0.8N, and the electronic supply layer 12 which consists of n form aluminum0.2Ga0.8N by which Si is doped as n form impurity. Each class 10, 11, and 12 of the semiconductor region 3 for components consists of the gallium nitride system compound semiconductor which used nitrogen and a gallium as the base. The electronic transit layer 10 contacted on a buffer layer 2 can also be called a channel layer, and has the thickness of 500nm. It controls that the spacer layer 11 arranged on the electronic transit layer 10 has the thickness of 7nm, and the silicon as an n form impurity of the electronic supply layer 12 diffuses it in the electronic transit layer 10. The electronic supply layer 12 arranged on the spacer layer 11 can also be called a barrier layer, a layer of operation, or a channel layer, and has the thickness of 10nm. The source electrode 4 and the drain electrode 5 carry out ohmic contact at the electronic supply layer 12, and are carrying out Schottky contact of the gate electrode 6 to the electronic supply layer 12. In addition, the high contact layer of n form high impurity concentration can be prepared between the source electrode 4 and the drain electrode 5, and the electronic supply layer

12. The insulator layer 7 which consists of SiO2 has covered the front face of a semiconductor region 10.
[0014] the electronic supply layer 12 and the spacer layer 11 -- **** -- since it is the thin film, it functions on a longitudinal direction as an insulating material, and functions on a lengthwise direction as a conductor. Therefore, at the time of actuation of HEMT, an electron flows in the path of the source electrode 4, the electronic supply layer 12, the spacer layer 11, the electronic transit layer 10, the spacer layer 11, the electronic supply layer 12, and the drain electrode 5. The flow of this electron, i.e., the flow of a current, is adjusted with the control voltage impressed to the gate electrode 6.
[0015] A substrate 1 consists of p form silicon single crystal which contains 3 group elements, such as B (boron), as an electric conduction form decision impurity. Principal plane 1a of the side by which the buffer layer 2 of this substrate 1 is arranged is a field just (111) in field bearing of the crystal shown with Miller indices. The high impurity concentration of this substrate 1 is a comparatively low value (about [for example, / 1x1013cm - three to 1x1016cm -] 3) in order to reduce the leakage current which passes along a substrate 1, and the resistivity of this substrate 1 is a comparatively high value, for example, 1.0 ohm-cm - 500 ohm-cm extent. A substrate 1 has the comparatively thick thickness of about 350 micrometers, and functions as a base material of a semiconductor region 3 and a buffer layer 2.
[0016] The buffer layer 2 arranged so that one whole principal plane of a substrate 1 may be covered consists of the compound layer to which the laminating of two or more 1st layers 8 and two or more 2nd layers 9 was carried out by turns. In drawing 1 , on account of illustration, although a part of buffer layer 2 is shown, a buffer layer 2 has the 1st 20 layer 8 and the 2nd 20 layer 9 in fact.
[0017] the 1st layer 8 -- chemical formula AlxGa1-xN -- it is here, and it comes out and x is formed with the numeric value of the arbitration which satisfies 0< x<=1, and the ingredient which can be shown. That is, the 1st layer 8 is formed by AlN (alumimium nitride) or AlGaN (gallium nitride aluminum). With drawing 1 and the operation gestalt of drawing 2 , AlN (alumimium nitride) by which x of said formula is equivalent to the ingredient set to 1 is used for the 1st layer 8. The 1st layer 8 is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of a layer 8 are closer to a silicon substrate 1 than the 2nd layer 9.
[0018] the 2nd layer 9 -- GaN (gallium nitride) or chemical formula AlyGa1-yN -- **** to which it is here, and it appears and y changes from y<x, the numeric value of arbitration with which are satisfied of 0< y<1, and the ingredient which can be shown -- it is the thin film. When using the semi-conductor which does not contain the electric conduction form decision impurity which consists of AlyGa1-yN as the 2nd layer 9, in order to prevent a crack with a possibility of generating according to increase of aluminum (aluminum), it is desirable to make y for it to be larger than the value, 0 [i.e.,], with which are satisfied of 0< y<0.8, and smaller than 0.8. In addition, the 2nd layer 9 of this 1st operation gestalt consists of GaN equivalent to y= 0 in the above-mentioned chemical formula. said 2nd layer -- chemical formula AlyGa1-yN -- the numeric value with which y is satisfied of y<x and 0<=y<1 here -- it can also come out and express.
[0019] The desirable thickness of the 1st layer 8 of a buffer layer 2 is 0.5nm - 50nm, i.e., 5-500A. When the thickness of the 1st layer 8 is less than 0.5nm, it becomes impossible to keep good the surface smoothness of the semiconductor region 3 for components formed in the top face of a buffer layer 2. When the thickness of the 1st layer 8 exceeds 50nm, a possibility that a crack may occur is in the 1st layer 8 by hauling distortion which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8.
[0020] The desirable thickness of the 2nd layer 9 is 0.5nm - 200nm, i.e., 5-2000A. When the thickness of the 2nd layer 9 is less than 0.5nm, it becomes difficult to grow up evenly the semiconductor region 3 for components which grows on the 1st layer 8 and a buffer layer 2. Moreover, if the thickness of the 2nd layer 9 exceeds 200nm, with the compressive stress which originates in the stacking fault of the 2nd layer 9 and the 1st layer 8, and is generated in the 2nd layer 9, the electron density of the channel layer 10 will fall and the property of HEMT will deteriorate. Furthermore, it is good preferably to make thickness of the 2nd layer 9 larger than the thickness of the 1st layer 8. If it does in this way, in holding down the distorted magnitude which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8 to extent which a crack does not generate in the 1st layer 9, and maintaining at the concentration-of-electrons high concentration of the channel layer 10, it will become advantageous.
[0021] Next, the manufacture approach of a semi-conductor semiconductor device that the 1st layer 8 was set to AlN and the 2nd layer 9 was set to GaN is explained.

[0022] First, the substrate 1 which consists of p form silicon semi-conductor with which p form impurity shown in (A) of drawing 3 was introduced is prepared. One principal plane 1a of the silicon substrate 1 for forming a buffer layer 2 is a field, i.e., an exact (111) field, just (111) in field bearing of the crystal shown with Miller indices. However, principal plane 1a of a substrate 1 can be made to incline in the range which is shown by 0 in drawing 3 (111) and which is just shown by -theta - +theta to a field. - The range of theta - +theta is -4 degrees - +4 degrees, is -3 degrees - +3 degrees preferably, and is -2 degrees - +2 degrees more preferably. losing the step in the atomic level at the time of carrying out epitaxial growth of a buffer layer 2 and the semiconductor region 3 for components by making just (111) crystal orientation of principal plane 1a of a silicon substrate 1 into a field or (111) the field from a field where an OFF include angle is small -- or it can be made small.
[0023] Next, as shown in drawing 3 (B), the buffer layer 2 on principal plane 1a of a substrate 1 is formed by repeating and carrying out the laminating of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of p form silicon single crystal pretreated by HF system etchant is arranged in the reaction chamber of an MOCVD system, first, thermal annealing for about 10 minutes is performed at 950 degrees C, and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas and NH3 (ammonia) gas are supplied for about 65 seconds in a reaction chamber, and the 1st layer 8 which changes from an AlN layer with a thickness of about 10nm to one principal plane of a substrate 1 is formed. After making whenever [stoving temperature / of a substrate 1] into 1120 degrees C in this example, it is about 63micromol/min and NH3 in the flow rate of TMA gas, i.e., the amount of supply of aluminum. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. Then, after making whenever [stoving temperature / of a substrate 1] into 1120 degrees C and stopping supply of TMA gas, it is TMG (trimethylgallium) gas and NH3 in a reaction chamber. Gas (ammonia) is supplied for about 90 seconds, and the 2nd layer 9 which consists of GaN of n form with a thickness of about 30nm is formed in the top face of the 1st layer 8 which consists of the above AlN formed in one principal plane of a substrate 1. At this example, it is about 60micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. In this example, 40 layers obtain the buffer layer 2 by which the laminating was carried out in the sum total of the 1st layer 8 which repeats formation of the 1st layer 8 which consists of above-mentioned AlN, and the 2nd layer 9 which consists of GaN 20 times, and consists of AlN, and the 2nd layer 9 which consists of GaN. The 1st layer 8 which consists of AlN, of course, and the 2nd layer 9 which consists of GaN are also changeable into the number of arbitration, such as 50 etc. layers, respectively.
[0024] next, MOCVD of common knowledge on the top face of a buffer layer 2 -- the form semiconductor region 3 for HEMT elements is formed by law. That is, the substrate 1 with which the buffer layer 2 was formed in the top face is arranged in the reaction chamber of an MOCVD system, and they are trimethylgallium gas, i.e., TMG gas, and NH3 first in a reaction chamber. The electronic transit layer 10 which consists of GaN which supplies gas (ammonia) for 15 minutes and does not include un-doping [with a thickness of about 500nm / GaN], i.e., an electric conduction form decision impurity, on the top face of a buffer layer 2 is formed. At this example, it is about 62micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, About 0.23 mols of amount of supply were set to /min.
[0025] Next, the spacer layer 11 which consists of aluminum0.2Ga0.8N which supplies TMG gas and ammonia gas to the TMA gas in a reaction chamber for 85 seconds, and does not include un-doping, i.e., an electric conduction form decision impurity, on the top face of the electronic transit layer 10 is formed in the thickness of 7nm. In this example, about 0.23 mols of flow rates of about 15micromol / min, and NH3 gas were set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to /min for the flow rate of about 8.4micromol/min and TMG gas.
[0026] Next, after interrupting crystal growth for about 15 seconds, the electronic supply layer 12 which supplies TMA gas, TMG gas, ammonia gas, and SiH4 (silane) gas for about 98 seconds in a reaction chamber, and changes from aluminum0.2Ga0.8N to the top face of the spacer layer 11 is formed in the thickness of about 10nm. In this example, about 0.23 mols of flow rates of /min and SiH4 gas were set [the flow rate of the TMA gas at this time / the flow rate of about 8.4micromol/min and TMG gas] to about 21 nmol(s) / min for the flow rate of about 15micromol / min, and ammonia gas.
[0027] Then, the silicon substrate 1 in which the semiconductor region 3 and the buffer layer 2 were formed is taken out from an MOCVD system, and the insulator layer 7 which consists of silicon oxide all over a semiconductor region 3 by well-known plasma CVD is formed. Thickness of an insulator layer 7 is set to about 100nm.

[0028] Although one HEMT is shown in drawing 1 , much HEMT(s) are made to coincidence using one semi-conductor wafer 1, i.e., substrate, at the time of this manufacture. For this reason, with photolithography, a semiconductor region 3 and the component isolation region of a buffer layer 2 are etched to a silicon substrate 1 by reactive ion etching using the mixed gas of 3 boron chloride (BCI3) and hydrogen, and isolation of HEMT is performed. Thus, if isolation is carried out, the electrical characteristics of each component field etc. can be inspected good, without being influenced of other components.
[0029] Next, after using photolithography and fluoric acid system etchant and forming opening for a source electrode and drain electrode formation in an insulator layer 7, using electron beam evaporation etc., laminating formation is carried out one by one, lift off of Ti (titanium) and the aluminum (aluminum) is carried out, and the source electrode 4 and the drain electrode 5 are formed. Also when forming a gate electrode, opening is formed in an insulator layer 7 in the same procedure, and the gate electrode 6 which vapor-deposits and carries out lift off of Pd (palladium), Ti (titanium), and the Au(gold) by electron beam evaporation, and has a function as a shot key barrier electrode is formed. Then, the semiconductor device (HEMT chip) which carried out cutting separation of the epitaxial wafer in the component isolation region, and turned the individual exception according to the well-known dicing process etc. is completed.
[0030] According to HEMT of this operation gestalt, the following effectiveness is acquired.
(1) Since the substrate 1 with which it is low cost and workability also consists of good silicon is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of HEMT is possible.
(2) The buffer layer 2 which consists of the 1st layer 8 to which the lattice constant formed in one principal plane of a substrate 1 changes from AlN which has a value between silicon and GaN, and the 2nd layer 9 can succeed the crystal orientation of the substrate 1 which consists of silicon good. Consequently, crystal orientation can be arranged and the GaN system semiconductor region 3 can be formed in one principal plane of a buffer layer 2 good. For this reason, the surface smoothness of a semiconductor region 3 becomes good, and the electrical characteristics of HEMT also become good. When a buffer layer is formed in one principal plane of the substrate 1 which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the GaN system semiconductor region excellent in surface smoothness in the top face of this buffer layer.
(3) As compared with the low-temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer 2 which consists of the compound layer of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer 2 does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase 3, i.e., a semiconductor region, formed on a buffer layer 2 can be made small enough, and generating of leakage current can be prevented. Consequently, HEMT with a good pinch-off property can be offered.
(4) Since a substrate 1 is formed from the silicon which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate 1, and many properties, such as pressure-proofing of a device and gain, are acquired good.
(5) a silicon substrate 1 -- a nitride system compound semiconductor -- comparing -- since a coefficient of thermal expansion is small -- heat -- it originated irregularly -- pull and distortion joins an epitaxial layer. For this reason, the tensile stress of the interface of AlGaN/GaN between the tooth-space layer 11 and the electronic transit layer 10 can be strengthened further, and the piezo electric field effect can be heightened as a result. For this reason, electron density of the electronic transit layer 10, i.e., a channel, can be made into high concentration as compared with HEMT which used silicon on sapphire, and it becomes possible to decrease the sheet resistance of the electronic transit layer 10, i.e., a channel, and to increase a drain current.
[0031]
[The 2nd operation gestalt] Next, MESFET of the 2nd operation gestalt is explained with reference to drawing 4 . However, in drawing 4 , the same sign is substantially given to the same part with drawing 1 R> 1, and the explanation is omitted. MESFET of drawing 4 prepares n type semiconductor field 3a which consists the semiconductor region 3 of HEMT of drawing 1 of the GaN compound semiconductor layer by which Si was doped as an n form impurity, and forms others identically to drawing 1 . That is, in MESFET of drawing 4 , a silicon substrate 1, a buffer layer 2, the source electrode 4, the drain electrode 5, the gate electrode 6, and the insulator layer 7 are formed like what is shown with the same sign by drawing 1 . N type semiconductor field 3a can also be called a channel layer or a barrier layer,

and is arranged on the buffer layer 2. The source electrode 4 and the gate electrode 5 carry out ohmic contact at n type semiconductor field 3a, and are carrying out shot key barrier contact of the gate electrode 6 at n type semiconductor field 3a.

[0032] The manufacture approaches other than GaN semiconductor region 3a of MESFET of drawing 4 are the same as that of the 1st operation gestalt. When forming GaN semiconductor region 3a, TMG gas, NH3 gas, and SiH4 (silane) gas are supplied for about 450 seconds in the reaction chamber used at the time of formation of a buffer layer 2, and with a thickness of about 150nm n type semiconductor field 3a is formed in the top face of the buffer layer 2 formed in one principal plane of a substrate 1. In this example, the flow rate of 0.23 mol/min and SiH4 gas, i.e., the amount of supply of Si, was made [the flow rate of TMG gas, i.e., the amount of supply of Ga] into 21 nmol/min for the flow rate of about 60micromol/min and NH3 gas, i.e., the amount of supply of NH3.

[0033] MESFET of drawing 4 has the same effectiveness as (1) stated in the column of explanation of the effectiveness of HEMT of drawing 1 , (2), (3), and (4). That is, it becomes possible to improve the surface smoothness of making a substrate 1 cheap and semiconductor region 3a, and crystallinity, to improve the property of MESFET, and to radiate the heat of semiconductor region 3a good through a silicon substrate 1.

[0034]

[The 3rd operation gestalt] The configuration of the buffer layer 2 of the 1st and 2nd operation gestalten is changeable. Drawing 5 shows a part of buffer layer 2a which follows the 3rd usable operation gestalt at HEMT, MESFET, etc. Buffer layer 2a of this drawing 5 consists of what carried out the laminating of the 2nd layer 9a of two or more 1st layer 8a and plurality by turns. 1st layer 8a -- chemical formula AlxInyGa1-x-yN -- it is here, and it comes out and x and y are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8a was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlInN (indium nitride aluminum), and AlGaInN (gallium nitride indium aluminum), and is formed. With the operation gestalt of drawing 5 , aluminum0.5In0.01Ga0.49N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0.01 is used for 1st layer 8a. **** in which 1st layer 8a has insulation -- it is the thin film. The 1st lattice constant and coefficient of thermal expansion containing aluminum of layer 8a have a value between the lattice constant of a silicon substrate 1 and a coefficient of thermal expansion, the lattice constant of semiconductor region 3a, and a coefficient of thermal expansion.

[0035] 2nd layer 9a -- chemical formula AlaInbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9a was chosen from GaN, AlN, InN, InGaN, AlGaN, AlInN, and AlInGaN, and is formed. With the operation gestalt of drawing 5 , aluminum0.05In0.35Ga0.6N equivalent to the ingredient with which a of said formula was set to 0.05, and b was set to 0.35 is used for 2nd layer 9a. It is larger than the band gap of 1st layer 8a, the gap, i.e., the band gap, between the valence band of 2nd layer 9a, and a conduction band.

[0036] Next, 1st layer 8a explains the manufacture approach of buffer layer 2a that aluminum0.5In0.01Ga0.49N and 2nd layer 9a were set to aluminum0.05In0.35Ga0.6N. Buffer layer 2a is formed on principal plane 1a of the same substrate 1 as the 1st operation gestalt. This buffer layer 2a is formed by repeating and carrying out the laminating of 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, and the 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, TMIn (trimethylindium) gas, and NH3 (ammonia) gas are supplied for about 24 seconds in a reaction chamber, and 1st layer 8a which changes from aluminum0.5In0.01Ga0.49N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 800 degrees C, the flow rate of 47micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas, i.e., the amount of supply of aluminum, / the flow rate of about 14micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 31micromol/min and TMIn gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas, TMG gas, and TMIn gas to 750 degrees C, TMA gas, TMG gas, TMIn gas, and NH3 (ammonia) gas are supplied for about 83 seconds after an appropriate time, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N whose thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8a. In

addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 59micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas / the flow rate of 2.8micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 46micromol/min and TMIn gas. In this example, 1st layer 8a which repeats formation of 1st layer 8a which consists of above-mentioned aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N 10 times, and consists of aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N form the buffer layer 2 by which the 20-layer laminating was carried out by turns. The 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, of course, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N are also changeable into the number of arbitration, such as 50 etc. layers, respectively.

[0037] Since buffer layer 2a of the 3rd operation gestalt of drawing 5 has the same effectiveness as the 1st operation gestalt of drawing 1 and the indium is further contained in buffer layer 2a, it has the effectiveness of the ability to make the coefficient of thermal expansion of buffer layer 2a approximate to a silicon substrate 1 rather than the case where an indium is not included in buffer layer 2a.

[0038]

[The 4th operation gestalt] Buffer layer 2b of the 4th operation gestalt shown in drawing 6 transforms the buffer layer 2 of drawing 1 and drawing 4 , and consists of the crosswise lamination object of the 1st and 2nd layers 8b and 9b. 1st layer 8b -- chemical formula AlxByGa1-x-yN -- it is here, and it comes out and x and y are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8b was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlBN (boron nitride aluminum), and AlBGaN (gallium nitride boron aluminum), and is formed. With the operation gestalt of drawing 6 , aluminum0.5Ga0.5N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0 is used for 1st layer 8b. 1st layer 8b is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of layer 8b are closer to a silicon substrate 1 than 2nd layer 9b.

[0039] 2nd layer 9b -- chemical formula AlaBbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9b is a layer containing at least one element chosen from aluminum, B, and Ga, and N, for example, was chosen from GaN, BN, AlN, BGaN, AlGaN, AlBN, and AlBGaN, and is formed. With the operation gestalt of drawing 6 , B0.3Ga0.7N equivalent to the ingredient with which a of said formula was set to 0 and b was set to 0.3 is used for 2nd layer 9b. It is larger than the band gap of 1st layer 8b, the gap, i.e., the band gap, between the valence band of 2nd layer 9b, and a conduction band.

[0040] Buffer layer 2b is formed by repeating and carrying out the laminating of 1st layer 8b which consists of aluminum0.5Ga0.5N, and the 2nd layer 9b which consists of B0.3Ga0.7N on principal plane 1a of a substrate 1 which has a field just (111), well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, and NH3 (ammonia) gas are supplied for about 27 seconds in a reaction chamber, and 1st layer 8b which changes from aluminum0.5Ga0.5N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 11 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 1080 degrees C, the flow rate of 31micromol/min and NH3 gas, i.e., the amount of supply of NH3, was set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to about 0.14 mols / min for the flow rate of about 31micromol/min and TMG gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas to 1120 degrees C, TEB (triethyl boron) gas, TMG gas, and NH3 (ammonia) gas are supplied for about 85 seconds after an appropriate time, and 2nd layer 9b which consists of B0.3Ga0.7N of n form where thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8b. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 63micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TEB gas, i.e., the amount of supply of boron,] into about 0.14 mol/min for the flow rate of 75micromol/min and TMG gas, i.e., the amount of supply of a gallium. In this example, 1st layer 8b which repeats formation of 2nd layer 9b which consists of the 1st layer 8b and B0.3Ga0.7N which consists of above-mentioned aluminum0.5Ga0.5N 50 times, and consists of aluminum0.5Ga0.5N, and 2nd layer 9b which consists of B0.3Ga0.7N form buffer layer 2b by which the 100-layer laminating was carried out by turns in total. 1st layer 8b which consists of aluminum0.5Ga0.5N, of course,

and 2nd layer 9b which consists of B0.3Ga0.7N are also changeable into the number of arbitration, such as 25 etc. layers, respectively.

[0041] Since buffer layer 2b of drawing 6 has the same effectiveness as the buffer layer 2 of drawing 1 and boron is further contained in 2nd layer 9b, compared with the case where 2nd layer 9b does not contain boron, it becomes strong, and has the effectiveness that generating of a crack can be prevented and 2nd layer 9b can be formed comparatively thickly.

[0042]

[Modification(s)] This invention is not limited to an above-mentioned operation gestalt, and the next deformation is possible for it.

(1) A substrate 11 can be used as silicon compounds, such as polycrystalline silicon other than single crystal silicon, or SiC.

(2) The electric conduction form of each class of semiconductor regions 3 and 3a can be made into an example and reverse.

(3) Each class of semiconductor regions 3 and 3a can be used as the gallium nitride system compound semiconductor or indium nitride system compound semiconductor chosen from GaN (gallium nitride), AlInN (indium nitride aluminum), AlGaN (gallium nitride aluminum), InGaN (gallium nitride indium), and AlInGaN (gallium nitride indium aluminum).

(4) In HEMT of drawing 1 , the electronic supply layer 12 and the same electronic supply layer can be prepared between a barrier layer 10, i.e., an electronic transit layer, and a buffer layer 2.

(5) The insulated-gate mold electrical quantity effectiveness transistor can be prepared instead of HEMT and MESFET.

(6) One layer can make [more] the number of buffer layers 2 and 2a and the 1st layers 8, 8a, and 8b of 2b than the 2nd layer 9, 9a, and 9b, and buffer layers 2 and 2a and the maximum upper layer of 2b can be used as the 1st layer 8, 8a, and 8b. Moreover, the one layer of the number of the 2nd layers 9, 9a, and 9b can also be conversely made [many] rather than the number of the 1st layers 8, 8a, and 8b.

(7) The 1st Layers 8, 8a, and 8b and 2nd layer 9, 9a, and 9b may contain an impurity in the range which does not check these functions.

[Translation done.]

* NOTICES *

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TECHNICAL FIELD

[Field of the Invention] This invention relates to a semiconductor device and its manufacture approaches, such as MESFET which used the nitride system compound semiconductor, and HEMT.
[0002]

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PRIOR ART

[Description of the Prior Art] Semiconductor devices, the metal semiconductor field-effect transistor (High Electron Mobility Transistor), i.e., MESFET (Metal Semiconductor Filed Effect Transistor) and a high electron mobility transistor, i.e., HEMT etc., using a gallium nitride system compound semiconductor etc., are well-known. in the semiconductor device using the conventional typical gallium nitride system compound semiconductor, it consists of about 500-600-degree C GaN or AlN comparatively formed at low-temperature substrate temperature on the insulating substrate which consists of sapphire -- it minds a low-temperature buffer layer (only henceforth a low-temperature buffer layer), and a compound semiconductor is formed.
[0003] That is, in forming MESFET, it forms on the insulating substrate which consists of sapphire, the layer of operation, i.e., the channel layer, which consists of the n form GaN layer which doped Si through the low-temperature buffer layer which consists of GaN or AlN, and forms a source electrode, a drain electrode, and a gate electrode in the front face of a layer of operation. Moreover, in forming HEMT, on the insulating substrate which consists of sapphire, the laminating of the electronic supply layer, the electronic transit layer, i.e., the channel layer, which consists of non-doping GaN through the low-temperature buffer layer which consists of GaN or AlN, which consists of the n form AlGaN is carried out, it is formed, and it forms a source electrode, a drain electrode, and a gate electrode in the front face of an electronic supply layer.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to invention of each claim, the following effectiveness is acquired.
(1) Since the substrate with which it is low cost and workability also consists of good silicon or a good silicon compound is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of a semiconductor device is possible.
(2) The buffer layer to which the lattice constant formed in one principal plane of a substrate changes from the 1st layer 8 which has a value between silicon and GaN, and the 2nd layer can succeed the crystal orientation of a substrate good. Consequently, crystal orientation can be arranged and a nitride system semiconductor region can be formed in one principal plane of a buffer layer good. For this reason, the surface smoothness of a semiconductor region becomes good and the electrical characteristics of a semiconductor device also become good. When a buffer layer is formed in one principal plane of the substrate which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the nitride system semiconductor region excellent in surface smoothness in the top face of this buffer layer.
(3) As compared with the low-temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer which consists of the compound layer of the 1st layer 8 and the 2nd layer 9 can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase, i.e., a semiconductor region, formed on a buffer layer can be made small enough, and generating of leakage current can be prevented.
(4) Since a substrate is formed from the silicon or the silicon compound which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate, and many properties, such as pressure-proofing of a device and gain, are acquired good. The indium is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 3. The stress relaxation effectiveness between the nitride system compound semiconductor (indium nitride system compound semiconductor) containing an indium, then a substrate and a nitride system semiconductor region is acquired still better at least in one side of the 1st and 2nd layers. That is, as compared with other nitride system compound semiconductors which do not contain In as a configuration element, for example, GaN, AlN, etc., the substrate and coefficient of thermal expansion which consist of silicon or a silicon compound approximate more the indium nitride system compound semiconductor which constitutes at least one side of the 1st and 2nd layers, for example, InN, InGaN, AlInN, AlInGaN, etc. For this reason, distortion of the semiconductor region resulting from the difference of the coefficient of thermal expansion between a substrate and a nitride system semiconductor region can be prevented good by including an indium in one [at least] layer among the 1st layer and the 2nd layer which constitute a buffer layer. B (boron) is contained in one [at least] layer of the 1st layer and the 2nd layer which constitute a buffer layer in invention of claim 4. The buffer layer containing B (boron) has a coefficient of thermal expansion near the coefficient of thermal expansion of the substrate which consists of silicon or a silicon compound rather than the buffer layer which does not have B (boron) **. For this reason, according to the buffer layer containing B (boron), distortion of the nitride system semiconductor region resulting from the coefficient-of-thermal-expansion difference between the substrates and nitride system semiconductor regions which consist of silicon or a silicon compound can be prevented good. In invention of claim 5, since the laminating of two or more 1st layers and two or more 2nd layers is carried out by turns and a buffer layer is constituted, two or more 1st thin layers are distributed. Consequently, buffer ability good as the

whole buffer layer can be obtained, and the crystallinity of the semiconductor region formed on a buffer layer becomes good. According to invention of claim 6, the buffer ability of a buffer layer can improve and surface smoothness of a nitride system semiconductor region can be improved. According to invention of claim 7, a buffer layer and a semiconductor region can be formed good on a substrate. namely, the thing abolished for the atomic step on the front face of a crystal of a buffer layer and a semiconductor region, i.e., the step in atomic level, by making field bearing of the principal plane of a substrate into a field or (111) the field from a field where an OFF include angle is small just (111) -- or it can lessen. If a buffer layer and a semiconductor region are formed on a principal plane with the large off include angle from a field just (111), it will see on atomic level to this etc., and a comparatively large step will arise. Although some steps do not become a problem so much when an epitaxial growth phase is comparatively thick, in the case of the semiconductor device which has the film of thickness, there is a possibility of causing the fall of a property. On the other hand, a field or the field where an off include angle is small, then a step become small just (111) about the principal plane of a substrate, and a buffer layer and a semiconductor region are formed good. According to invention of claim 12, a semiconductor device with a sufficient property can be formed cheaply and easily.

[0011]

[The 1st operation gestalt] Next, HEMT using the gallium nitride system compound semiconductor applied to the 1st operation gestalt of this invention with reference to drawing 1 - drawing 3 is explained.

[0012] HEMT concerning the 1st operation gestalt of this invention shown in drawing 1 consists of a buffer layer, the substrate 1, i.e., the substrate, which consists of silicon, 2, the semiconductor region 3 for HEMT elements, the source electrode 4 as the 1st electrode, the drain electrode 5 as the 2nd electrode, the gate electrode 6 as a control electrode, and an insulator layer 7.

[0013] The HEMT element semiconductor region 3 has the electronic transit layer 10 which consists of impurity non-doping GaN, the spacer layer 11 which consists of non-doping aluminum0.2Ga0.8N, and the electronic supply layer 12 which consists of n form aluminum0.2Ga0.8N by which Si is doped as an n form impurity. Each class 10, 11, and 12 of the semiconductor region 3 for components consists of the gallium nitride system compound semiconductor which used nitrogen and a gallium as the base. The electronic transit layer 10 arranged on a buffer layer 2 can also be called a channel layer, and has the thickness of 500nm. It controls that the spacer layer 11 arranged on the electronic transit layer 10 has the thickness of 7nm, and the silicon as an n form impurity of the electronic supply layer 12 diffuses it in the electronic transit layer 10. The electronic supply layer 12 arranged on the spacer layer 11 can also be called a barrier layer, a layer of operation, or a channel layer, and has the thickness of 10nm. The source electrode 4 and the drain electrode 5 carry out ohmic contact at the electronic supply layer 12, and are carrying out Schottky contact of the gate electrode 6 to the electronic supply layer 12. In addition, the high contact layer of n form high impurity concentration can be prepared between the source electrode 4 and the drain electrode 5, and the electronic supply layer 12. The insulator layer 7 which consists of SiO2 has covered the front face of a semiconductor region 10.

[0014] the electronic supply layer 12 and the spacer layer 11 -- **** -- since it is the thin film, it functions on a longitudinal direction as an insulating material, and functions on a lengthwise direction as a conductor. Therefore, at the time of actuation of HEMT, an electron flows in the path of the source electrode 4, the electronic supply layer 12, the spacer layer 11, the electronic transit layer 10, the spacer layer 11, the electronic supply layer 12, and the drain electrode 5. The flow of this electron, i.e., the flow of a current, is adjusted with the control voltage impressed to the gate electrode 6.

[0015] A substrate 1 consists of p form silicon single crystal which contains 3 group elements, such as B (boron), as an electric conduction form decision impurity. Principal plane 1a of the side by which the buffer layer 2 of this substrate 1 is arranged is a field just (111) in field bearing of the crystal shown with Miller indices. The high impurity concentration of this substrate 1 is a comparatively low value (about [for example, / 1x1013cm - three to 1x1016cm -] 3) in order to reduce the leakage current which passes along a substrate 1, and the resistivity of this substrate 1 is a comparatively high value, for example, 1.0 ohm-cm - 500 ohm-cm extent. A substrate 1 has the comparatively thick thickness of about 350 micrometers, and functions as a base material of a semiconductor region 3 and a buffer layer 2.

[0016] The buffer layer 2 arranged so that one whole principal plane of a substrate 1 may be covered consists of the compound layer to which the laminating of two or more 1st layers 8 and two or more 2nd layers 9 was carried out by turns. In drawing 1 , on account of illustration, although a part of buffer layer 2 is shown, a buffer layer 2 has the 1st 20 layer 8 and the 2nd 20 layer 9 in fact.

[0017] the 1st layer 8 -- chemical formula AlxGa1-xN -- it is here, and it comes out and x is formed with the numeric

value of the arbitration which satisfies 0< x<=1, and the ingredient which can be shown. That is, the 1st layer 8 is formed by AlN (alumimium nitride) or AlGaN (gallium nitride aluminum). With drawing 1 and the operation gestalt of drawing 2 , AlN (alumimium nitride) by which x of said formula is equivalent to the ingredient set to 1 is used for the 1st layer 8. The 1st layer 8 is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of a layer 8 are closer to a silicon substrate 1 than the 2nd layer 9.

[0018] the 2nd layer 9 -- GaN (gallium nitride) or chemical formula AlyGa1-yN -- **** to which it is here, and it appears and y changes from y<x, the numeric value of arbitration with which are satisfied of 0< y<1, and the ingredient which can be shown -- it is the thin film. When using the semi-conductor which does not contain the electric conduction form decision impurity which consists of AlyGa1-yN as the 2nd layer 9, in order to prevent a crack with a possibility of generating according to increase of aluminum (aluminum), it is desirable to make y for it to be larger than the value, 0 [i.e.,], with which are satisfied of 0< y<0.8, and smaller than 0.8. In addition, the 2nd layer 9 of this 1st operation gestalt consists of GaN equivalent to y= 0 in the above-mentioned chemical formula. said 2nd layer -- chemical formula AlyGa1-yN -- the numeric value with which y is satisfied of y<x and 0<=y<1 here -- it can also come out and express.

[0019] The desirable thickness of the 1st layer 8 of a buffer layer 2 is 0.5nm - 50nm, i.e., 5-500A. When the thickness of the 1st layer 8 is less than 0.5nm, it becomes impossible to keep good the surface smoothness of the semiconductor region 3 for components formed in the top face of a buffer layer 2. When the thickness of the 1st layer 8 exceeds 50nm, a possibility that a crack may occur is in the 1st layer 8 by hauling distortion which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8.

[0020] The desirable thickness of the 2nd layer 9 is 0.5nm - 200nm, i.e., 5-2000A. When the thickness of the 2nd layer 9 is less than 0.5nm, it becomes difficult to grow up evenly the semiconductor region 3 for components which grows on the 1st layer 8 and a buffer layer 2. Moreover, if the thickness of the 2nd layer 9 exceeds 200nm, with the compressive stress which originates in the stacking fault of the 2nd layer 9 and the 1st layer 8, and is generated in the 2nd layer 9, the electron density of the channel layer 10 will fall and the property of HEMT will deteriorate. Furthermore, it is good preferably to make thickness of the 2nd layer 9 larger than the thickness of the 1st layer 8. If it does in this way, in holding down the distorted magnitude which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8 to extent which a crack does not generate in the 1st layer 9, and maintaining at the concentration-of-electrons high concentration of the channel layer 10, it will become advantageous.

[0021] Next, the manufacture approach of a semi-conductor semiconductor device that the 1st layer 8 was set to AlN and the 2nd layer 9 was set to GaN is explained.

[0022] First, the substrate 1 which consists of p form silicon semi-conductor with which p form impurity shown in (A) of drawing 3 was introduced is prepared. One principal plane 1a of the silicon substrate 1 for forming a buffer layer 2 is a field, i.e., an exact (111) field, just (111) in field bearing of the crystal shown with Miller indices. However, principal plane 1a of a substrate 1 can be made to incline in the range which is shown by 0 in drawing 3 (111) and which is just shown by -theta - +theta to a field. - The range of theta - +theta is -4 degrees - +4 degrees, is -3 degrees - +3 degrees preferably, and is -2 degrees - +2 degrees more preferably. losing the step in the atomic level at the time of carrying out epitaxial growth of a buffer layer 2 and the semiconductor region 3 for components by making just (111) crystal orientation of principal plane 1a of a silicon substrate 1 into a field or (111) the field from a field where an OFF include angle is small -- or it can be made small.

[0023] Next, as shown in drawing 3 (B), the buffer layer 2 on principal plane 1a of a substrate 1 is formed by repeating and carrying out the laminating of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of p form silicon single crystal pretreated by HF system etchant is arranged in the reaction chamber of an MOCVD system, first, thermal annealing for about 10 minutes is performed at 950 degrees C, and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas and NH3 (ammonia) gas are supplied for about 65 seconds in a reaction chamber, and the 1st layer 8 which changes from an AlN layer with a thickness of about 10nm to one principal plane of a substrate 1 is formed. After making whenever [stoving temperature / of a substrate 1] into 1120 degrees C in this example, it is about 63micromol/min and NH3 in the flow rate of TMA gas, i.e., the amount of supply of aluminum. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. Then,

after making whenever [stoving temperature / of a substrate 1] into 1120 degrees C and stopping supply of TMA gas, it is TMG (trimethylgallium) gas and NH3 in a reaction chamber. Gas (ammonia) is supplied for about 90 seconds, and the 2nd layer 9 which consists of GaN of n form with a thickness of about 30nm is formed in the top face of the 1st layer 8 which consists of the above AlN formed in one principal plane of a substrate 1. At this example, it is about 60micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, The amount of supply was made into about 0.14 mol/min. In this example, 40 layers obtain the buffer layer 2 by which the laminating was carried out in the sum total of the 1st layer 8 which repeats formation of the 1st layer 8 which consists of above-mentioned AlN, and the 2nd layer 9 which consists of GaN 20 times, and consists of AlN, and the 2nd layer 9 which consists of GaN. The 1st layer 8 which consists of AlN, of course, and the 2nd layer 9 which consists of GaN are also changeable into the number of arbitration, such as 50 etc. layers, respectively.

[0024] next, MOCVD of common knowledge on the top face of a buffer layer 2 -- the form semiconductor region 3 for HEMT elements is formed by law. That is, the substrate 1 with which the buffer layer 2 was formed in the top face is arranged in the reaction chamber of an MOCVD system, and they are trimethylgallium gas, i.e., TMG gas, and NH3 first in a reaction chamber. The electronic transit layer 10 which consists of GaN which supplies gas (ammonia) for 15 minutes and does not include un-doping [with a thickness of about 500nm / GaN], i.e., an electric conduction form decision impurity, on the top face of a buffer layer 2 is formed. At this example, it is about 62micromol/min and NH3 in the flow rate of TMG gas, i.e., the amount of supply of Ga. Flow rate 3 of gas, i.e., NH, About 0.23 mols of amount of supply were set to /min.

[0025] Next, the spacer layer 11 which consists of aluminum0.2Ga0.8N which supplies TMG gas and ammonia gas to the TMA gas in a reaction chamber for 85 seconds, and does not include un-doping, i.e., an electric conduction form decision impurity, on the top face of the electronic transit layer 10 is formed in the thickness of 7nm. In this example, about 0.23 mols of flow rates of about 15micromol / min, and NH3 gas were set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to /min for the flow rate of about 8.4micromol/min and TMG gas.

[0026] Next, after interrupting crystal growth for about 15 seconds, the electronic supply layer 12 which supplies TMA gas, TMG gas, ammonia gas, and SiH4 (silane) gas for about 98 seconds in a reaction chamber, and changes from aluminum0.2Ga0.8N to the top face of the spacer layer 11 is formed in the thickness of about 10nm. In this example, about 0.23 mols of flow rates of /min and SiH4 gas were set [the flow rate of the TMA gas at this time / the flow rate of about 8.4micromol/min and TMG gas] to about 21 nmol(s) / min for the flow rate of about 15micromol / min, and ammonia gas.

[0027] Then, the silicon substrate 1 in which the semiconductor region 3 and the buffer layer 2 were formed is taken out from an MOCVD system, and the insulator layer 7 which consists of silicon oxide all over a semiconductor region 3 by well-known plasma CVD is formed. Thickness of an insulator layer 7 is set to about 100nm.

[0028] Although one HEMT is shown in drawing 1 , much HEMT(s) are made to coincidence using one semiconductor wafer 1, i.e., substrate, at the time of this manufacture. For this reason, with photolithography, a semiconductor region 3 and the component isolation region of a buffer layer 2 are etched to a silicon substrate 1 by reactive ion etching using the mixed gas of 3 boron chloride (BCI3) and hydrogen, and isolation of HEMT is performed. Thus, if isolation is carried out, the electrical characteristics of each component field etc. can be inspected good, without being influenced of other components.

[0029] Next, after using photolithography and fluoric acid system etchant and forming opening for a source electrode and drain electrode formation in an insulator layer 7, using electron beam evaporation etc., laminating formation is carried out one by one, lift off of Ti (titanium) and the aluminum (aluminum) is carried out, and the source electrode 4 and the drain electrode 5 are formed. Also when forming a gate electrode, opening is formed in an insulator layer 7 in the same procedure, and the gate electrode 6 which vapor-deposits and carries out lift off of Pd (palladium), Ti (titanium), and the Au(gold) by electron beam evaporation, and has a function as a shot key barrier electrode is formed. Then, the semiconductor device (HEMT chip) which carried out cutting separation of the epitaxial wafer in the component isolation region, and turned the individual exception according to the well-known dicing process etc. is completed.

[0030] According to HEMT of this operation gestalt, the following effectiveness is acquired.

(1) Since the substrate 1 with which it is low cost and workability also consists of good silicon is used, reduction of ingredient cost and a production cost is possible. For this reason, the cost reduction of HEMT is possible.

(2) The buffer layer 2 which consists of the 1st layer 8 to which the lattice constant formed in one principal plane of a

substrate 1 changes from AlN which has a value between silicon and GaN, and the 2nd layer 9 can succeed the crystal orientation of the substrate 1 which consists of silicon good. Consequently, crystal orientation can be arranged and the GaN system semiconductor region 3 can be formed in one principal plane of a buffer layer 2 good. For this reason, the surface smoothness of a semiconductor region 3 becomes good, and the electrical characteristics of HEMT also become good. When a buffer layer is formed in one principal plane of the substrate 1 which consists of silicon at low temperature only with a GaN semi-conductor, since the difference of a lattice constant is large, silicon and GaN cannot form the GaN system semiconductor region excellent in surface smoothness in the top face of this buffer layer.
(3) As compared with the low-temperature buffer layer which consists of conventional GaN and a monolayer of AlN, crystal growth of the buffer layer 2 which consists of the compound layer of the 1st layer 8 which consists of AlN, and the 2nd layer 9 which consists of GaN can be carried out at an elevated temperature. For this reason, the ammonia used as a nitrogen source can be made to disassemble good, and a buffer layer 2 does not turn into an amorphous layer. For this reason, the consistency of the crystal defect of the epitaxial growth phase 3, i.e., a semiconductor region, formed on a buffer layer 2 can be made small enough, and generating of leakage current can be prevented. Consequently, HEMT with a good pinch-off property can be offered.
(4) Since a substrate 1 is formed from the silicon which is excellent in the heat conductivity as compared with sapphire, the heat generated working [a device] can be made to radiate heat good through a substrate 1, and many properties, such as pressure-proofing of a device and gain, are acquired good.
(5) a silicon substrate 1 -- a nitride system compound semiconductor -- comparing -- since a coefficient of thermal expansion is small -- heat -- it originated irregularly -- pull and distortion joins an epitaxial layer. For this reason, the tensile stress of the interface of AlGaN/GaN between the tooth-space layer 11 and the electronic transit layer 10 can be strengthened further, and the piezo electric field effect can be heightened as a result. For this reason, electron density of the electronic transit layer 10, i.e., a channel, can be made into high concentration as compared with HEMT which used silicon on sapphire, and it becomes possible to decrease the sheet resistance of the electronic transit layer 10, i.e., a channel, and to increase a drain current.
[0031]
[The 2nd operation gestalt] Next, MESFET of the 2nd operation gestalt is explained with reference to drawing 4 . However, in drawing 4 , the same sign is substantially given to the same part with drawing 1 ,R> 1, and the explanation is omitted. MESFET of drawing 4 prepares n type semiconductor field 3a which consists the semiconductor region 3 of HEMT of drawing 1 of the GaN compound semiconductor layer by which Si was doped as an n form impurity, and forms others identically to drawing 1 . That is, in MESFET of drawing 4 , a silicon substrate 1, a buffer layer 2, the source electrode 4, the drain electrode 5, the gate electrode 6, and the insulator layer 7 are formed like what is shown with the same sign by drawing 1 . N type semiconductor field 3a can also be called a channel layer or a barrier layer, and is arranged on the buffer layer 2. The source electrode 4 and the gate electrode 5 carry out ohmic contact at n type semiconductor field 3a, and are carrying out shot key barrier contact of the gate electrode 6 at n type semiconductor field 3a.
[0032] The manufacture approaches other than GaN semiconductor region 3a of MESFET of drawing 4 are the same as that of the 1st operation gestalt. When forming GaN semiconductor region 3a, TMG gas, NH3 gas, and SiH4 (silane) gas are supplied for about 450 seconds in the reaction chamber used at the time of formation of a buffer layer 2, and with a thickness of about 150nm n type semiconductor field 3a is formed in the top face of the buffer layer 2 formed in one principal plane of a substrate 1. In this example, the flow rate of 0.23 mol/min and SiH4 gas, i.e., the amount of supply of Si, was made [the flow rate of TMG gas, i.e., the amount of supply of Ga] into 21 nmol/min for the flow rate of about 60micromol/min and NH3 gas, i.e., the amount of supply of NH3.
[0033] MESFET of drawing 4 has the same effectiveness as (1) stated in the column of explanation of the effectiveness of HEMT of drawing 1 , (2), (3), and (4). That is, it becomes possible to improve the surface smoothness of making a substrate 1 cheap and semiconductor region 3a, and crystallinity, to improve the property of MESFET, and to radiate the heat of semiconductor region 3a good through a silicon substrate 1.
[0034]
[The 3rd operation gestalt] The configuration of the buffer layer 2 of the 1st and 2nd operation gestalten is changeable. Drawing 5 shows a part of buffer layer 2a which follows the 3rd usable operation gestalt at HEMT, MESFET, etc. Buffer layer 2a of this drawing 5 consists of what carried out the laminating of the 2nd layer 9a of two or more 1st layer 8a and plurality by turns. 1st layer 8a -- chemical formula AlxInyGa1-x-yN -- it is here, and it comes out and x and y

are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8a was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlInN (indium nitride aluminum), and AlGaInN (gallium nitride indium aluminum), and is formed. With the operation gestalt of drawing 5 , aluminum0.5In0.01Ga0.49N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0.01 is used for 1st layer 8a. **** in which 1st layer 8a has insulation -- it is the thin film. The 1st lattice constant and coefficient of thermal expansion containing aluminum of layer 8a have a value between the lattice constant of a silicon substrate 1 and a coefficient of thermal expansion, the lattice constant of semiconductor region 3a, and a coefficient of thermal expansion.

[0035] 2nd layer 9a -- chemical formula AlaInbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9a was chosen from GaN, AlN, InN, InGaN, AlGaN, AlInN, and AlInGaN, and is formed. With the operation gestalt of drawing 5 , aluminum0.05In0.35Ga0.6N equivalent to the ingredient with which a of said formula was set to 0.05, and b was set to 0.35 is used for 2nd layer 9a. It is larger than the band gap of 1st layer 8a, the gap, i.e., the band gap, between the valence band of 2nd layer 9a, and a conduction band.

[0036] Next, 1st layer 8a explains the manufacture approach of buffer layer 2a that aluminum0.5In0.01Ga0.49N and 2nd layer 9a were set to aluminum0.05In0.35Ga0.6N. Buffer layer 2a is formed on principal plane 1a of the same substrate 1 as the 1st operation gestalt. This buffer layer 2a is formed by repeating and carrying out the laminating of 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, and the 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, TMIn (trimethylindium) gas, and NH3 (ammonia) gas are supplied for about 24 seconds in a reaction chamber, and 1st layer 8a which changes from aluminum0.5In0.01Ga0.49N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 800 degrees C, the flow rate of 47micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas, i.e., the amount of supply of aluminum, / the flow rate of about 14micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 31micromol/min and TMIn gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas, TMG gas, and TMIn gas to 750 degrees C, TMA gas, TMG gas, TMIn gas, and NH3 (ammonia) gas are supplied for about 83 seconds after an appropriate time, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N whose thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8a. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 59micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas / the flow rate of 2.8micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 46micromol/min and TMIn gas. In this example, 1st layer 8a which repeats formation of 1st layer 8a which consists of above-mentioned aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N 10 times, and consists of aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N form the buffer layer 2 by which the 20-layer laminating was carried out by turns. The 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, of course, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N are also changeable into the number of arbitration, such as 50 etc. layers, respectively.

[0037] Since buffer layer 2a of the 3rd operation gestalt of drawing 5 has the same effectiveness as the 1st operation gestalt of drawing 1 and the indium is further contained in buffer layer 2a, it has the effectiveness of the ability to make the coefficient of thermal expansion of buffer layer 2a approximate to a silicon substrate 1 rather than the case where an indium is not included in buffer layer 2a.

[0038]

[The 4th operation gestalt] Buffer layer 2b of the 4th operation gestalt shown in drawing 6 transforms the buffer layer 2 of drawing 1 and drawing 4 , and consists of the crosswise lamination object of the 1st and 2nd layers 8b and 9b. 1st layer 8b -- chemical formula AlxByGa1-x-yN -- it is here, and it comes out and x and y are formed with the numeric value of the arbitration which satisfies 0< x<=1, 0<=y<1, and x+y<=1, and the ingredient which can be shown. That is, 1st layer 8b was chosen from AlN (alumimium nitride), AlGaN (gallium nitride aluminum), AlBN (boron nitride

aluminum), and AlBGaN (gallium nitride boron aluminum), and is formed. With the operation gestalt of drawing 6 , aluminum0.5Ga0.5N equivalent to the ingredient with which x of said formula was set to 0.5, and y was set to 0 is used for 1st layer 8b. 1st layer 8b is very thin film which has insulation. The 1st lattice constant and coefficient of thermal expansion of layer 8b are closer to a silicon substrate 1 than 2nd layer 9b.

[0039] 2nd layer 9b -- chemical formula AlaBbGa1-a-bN -- it is here and a and b are the numeric value of the arbitration which satisfies 0<=a<1, 0<=b<1, and a+b<=1, and the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9b is a layer containing at least one element chosen from aluminum, B, and Ga, and N, for example, was chosen from GaN, BN, AlN, BGaN, AlGaN, AlBN, and AlBGaN, and is formed. With the operation gestalt of drawing 6 , B0.3Ga0.7N equivalent to the ingredient with which a of said formula was set to 0 and b was set to 0.3 is used for 2nd layer 9b. It is larger than the band gap of 1st layer 8b, the gap, i.e., the band gap, between the valence band of 2nd layer 9b, and a conduction band.

[0040] Buffer layer 2b is formed by repeating and carrying out the laminating of 1st layer 8b which consists of aluminum0.5Ga0.5N, and the 2nd layer 9b which consists of B0.3Ga0.7N on principal plane 1a of a substrate 1 which has a field just (111), well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, and NH3 (ammonia) gas are supplied for about 27 seconds in a reaction chamber, and 1st layer 8b which changes from aluminum0.5Ga0.5N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 11 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 1080 degrees C, the flow rate of 31micromol/min and NH3 gas, i.e., the amount of supply of NH3, was set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to about 0.14 mols / min for the flow rate of about 31micromol/min and TMG gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas to 1120 degrees C, TEB (triethyl boron) gas, TMG gas, and NH3 (ammonia) gas are supplied for about 85 seconds after an appropriate time, and 2nd layer 9b which consists of B0.3Ga0.7N of n form where thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8b. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 63micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TEB gas, i.e., the amount of supply of boron,] into about 0.14 mol/min for the flow rate of 75micromol/min and TMG gas, i.e., the amount of supply of a gallium. In this example, 1st layer 8b which repeats formation of 2nd layer 9b which consists of the 1st layer 8b and B0.3Ga0.7N which consists of above-mentioned aluminum0.5Ga0.5N 50 times, and consists of aluminum0.5Ga0.5N, and 2nd layer 9b which consists of B0.3Ga0.7N form buffer layer 2b by which the 100-layer laminating was carried out by turns in total. 1st layer 8b which consists of aluminum0.5Ga0.5N, of course, and 2nd layer 9b which consists of B0.3Ga0.7N are also changeable into the number of arbitration, such as 25 etc. layers, respectively.

[0041] Since buffer layer 2b of drawing 6 has the same effectiveness as the buffer layer 2 of drawing 1 and boron is further contained in 2nd layer 9b, compared with the case where 2nd layer 9b does not contain boron, it becomes strong, and has the effectiveness that generating of a crack can be prevented and 2nd layer 9b can be formed comparatively thickly.

[0042]

[Modification(s)] This invention is not limited to an above-mentioned operation gestalt, and the next deformation is possible for it.

(1) A substrate 11 can be used as silicon compounds, such as polycrystalline silicon other than single crystal silicon, or SiC.

(2) The electric conduction form of each class of semiconductor regions 3 and 3a can be made into an example and reverse.

(3) Each class of semiconductor regions 3 and 3a can be used as the gallium nitride system compound semiconductor or indium nitride system compound semiconductor chosen from GaN (gallium nitride), AlInN (indium nitride aluminum), AlGaN (gallium nitride aluminum), InGaN (gallium nitride indium), and AlInGaN (gallium nitride indium aluminum).

(4) In HEMT of drawing 1 , the electronic supply layer 12 and the same electronic supply layer can be prepared between a barrier layer 10, i.e., an electronic transit layer, and a buffer layer 2.

(5) The insulated-gate mold electrical quantity effectiveness transistor can be prepared instead of HEMT and MESFET.

(6) One layer can make [more] the number of buffer layers 2 and 2a and the 1st layers 8, 8a, and 8b of 2b than the 2nd layer 9, 9a, and 9b, and buffer layers 2 and 2a and the maximum upper layer of 2b can be used as the 1st layer 8, 8a, and 8b. Moreover, the one layer of the number of the 2nd layers 9, 9a, and 9b can also be conversely made [many] rather than the number of the 1st layers 8, 8a, and 8b.
(7) The 1st Layers 8, 8a, and 8b and 2nd layer 9, 9a, and 9b may contain an impurity in the range which does not check these functions.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, this kind of a gallium nitride system or a nitride system semiconductor device cuts down the wafer which many components made as everyone knows and was full according to dicing, scribing, a cleavage (cleavage), etc., and is formed. Since the insulating substrate which consists of sapphire at this time had the high degree of hardness, it was difficult to perform this dicing etc. with sufficient productivity. Moreover, since sapphire was expensive, the cost of a semiconductor device became high. Moreover, when carrying out crystal growth of the nitride system compound semiconductor on silicon on sapphire, in order to obtain a flat nitride system compound semiconductor layer, it is necessary to form a low-temperature buffer layer as mentioned above. If crystal growth of the nitride system compound semiconductor layer is carried out at an elevated temperature through a low-temperature buffer layer, the comparatively flat nitride system compound semiconductor film can be formed on silicon on sapphire. However, at low temperature, when the low-temperature buffer layer which consists of GaN or AlN is formed, since the ammonia used as a nitrogen source hardly disassembles, a low-temperature buffer layer becomes an amorphous layer containing metal-like Ga and aluminum. Since crystal growth of a channel layer, i.e., the layer of operation etc., is carried out on the buffer layer of this amorphous condition, in the field near a low-temperature buffer layer, the consistency of a crystal defect becomes very high. Since the high field of this defect density functions as an n type semiconductor layer of low resistance, when operating a device, a current leaks it also to this n type semiconductor layer in addition to a layer (channel layer) of operation. Consequently, a good pinch-off property is no longer acquired. As an approach of solving this problem, an AlGaN layer is made to intervene between a buffer layer and a channel layer, and the technique of controlling current leak in a low resistance n type semiconductor layer is proposed by JP,2000-299325,A. However, in order that mediation of an AlGaN layer may generate distortion which originated in the epitaxial layer at the stacking fault, it reduces the electron mobility of a channel layer and invites the problem of making a channel layer generate a crack further etc. For this reason, it was difficult to restrain Al amount and thickness of an AlGaN layer and to fully control leakage current as a result.
[0005] Moreover, the heat conductivity of silicon on sapphire could not fully emit the heat generated working [a device] since it is small, 0.126 W/cm-K and, but caused the fall of many properties of a transistor, such as reducing pressure-proofing, gain, etc. of a device. Furthermore, although the hetero structure which carried out the laminating of the AlGaN is generally adopted on the GaN layer by the GaN system HEMT, when growing up AlGaN on a GaN layer, a stacking fault pulls to the field inboard in AlGaN, and distortion is generated. For this stress, piezo polarization electric field occur in an interface, and if it combines with spontaneous polarization, the electric field of several MV/cm will occur in a hetero interface. Into a channel, it is accumulated by this electric field, the two-dimensional electron gas EG, i.e., 2D, of 1013cm-2 order, the fall of channel sheet resistance is achieved, and a drain current can be made to increase. This is the advantage of the GaN system HEMT which adopted the hetero structure which carried out the laminating of the AlGaN on the GaN layer.
[0006] however, silicon on sapphire -- since a coefficient of thermal expansion is larger than a nitride system compound semiconductor -- heat -- therefore, an epitaxial layer is made to generate a compressive strain irregularly Since this compressive strain works in the direction which cancels the hauling distortion in AlGaN resulting from a stacking fault, it will decrease piezo polarization electric field. For this reason, the concentration of electrons of 2D EG also falls and the engine performance of the AlGaN/GaN system HEMT cannot fully be demonstrated.
[0007] Then, the purpose of this invention is to offer a semiconductor device and its manufacture approaches, such as MESFET using the nitride system compound semiconductor which can solve an above-mentioned trouble, and HEMT.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] This invention for solving the above-mentioned technical problem and attaining the above-mentioned purpose The substrate which is the semiconductor device which has a nitride system compound semiconductor, and consists of silicon or a silicon compound, The semiconductor region for semiconductor devices containing at least one nitride system compound semiconductor layer which has been arranged on one principal plane of said substrate, and has been arranged on a buffer layer and said buffer layer, the 1st main electrode, 2nd main electrode, and control electrode which have been arranged on the front face of said semiconductor region for semiconductor devices -- having -- said buffer layer -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which it is here and said M was chosen from In (indium) and B (boron),

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula AlaMbGa1-a-bN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

前記a及びbは、 $0\leqq a\leqq 1$、
$0\leqq b<1$、
$a+b\leqq 1$

the numeric value to satisfy and the semiconductor device characterized by consisting of a compound layer with the 2nd layer which comes out and consists of the ingredient shown are started.
[0009] In addition, as shown in claim 2, said 1st layer can be set to AlxGa1-xN, and said 2nd layer can be set to AlaGa1-aN. Moreover, as shown in claim 3, said 1st layer can be made into AlxInyGa1-x-yN, said 2nd layer can be made into AlaInbGa1-a-bN, and In (indium) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 4, said 1st layer can be made into AlxByGa1-x-yN, said 2nd layer can be made into AlaBbGa1-a-bN, and B (boron) can be included at least in one side of said 1st and 2nd layers. Moreover, as shown in claim 5, as for said buffer layer, it is desirable to consist of said two or more 1st and 2nd layers, and to carry out the laminating of said the 1st layer and said 2nd layer by turns. Moreover, as shown in claim 6, it is desirable for the thickness of said 1st layer in said buffer layer to be [for the thickness of 0.5nm - 50nm and said 2nd layer] 0.5nm - 200nm. As shown in claim 7, as for the principal plane of the side by which said buffer layer of said substrate is arranged, it is desirable that it is the field to which it leans in -4 to +4 times from the field or (111) the field just (111) in field bearing of the crystal shown with Miller indices. Moreover, as shown in claim 8, as for said nitride system compound semiconductor layer, it is desirable to be chosen from a GaN (gallium nitride) layer, an AlInN (indium nitride aluminum) layer, an AlGaN (gallium nitride aluminum) layer, an InGaN (gallium nitride indium) layer, and an AlInGaN (gallium nitride indium aluminum) layer. Moreover, as shown in claim 9, said semiconductor region can be used as two or more semi-conductor layers for forming a field-effect transistor, said 1st main electrode can be used as a source electrode, said 2nd main electrode can be used as a drain electrode, and said control electrode can be used as a gate electrode. Moreover, as shown in claim 10, said semiconductor region can be used as two or more semi-conductor layers for forming a high electron mobility transistor (HEMT). Moreover, as shown in claim 11, said semiconductor region can be used as two or

more semi-conductor layers for forming a metal semiconductor field-effect transistor (MESFET). moreover, the process which prepares the substrate which consists of silicon or a silicon compound in the manufacture approach of a semiconductor device of having a nitride system compound semiconductor as shown in claim 12 and said substrate top -- vapor growth -- chemical formula AlxMyGa1-x-yN -- at least one sort of elements with which said M was chosen from In (indium) and B (boron) here,

前記x及びyは、 $0<x\leqq 1$、
$0\leqq y<1$、
$x+y\leqq 1$

the numeric value to satisfy, the 1st layer which comes out and consists of the ingredient shown, and chemical formula At least one sort of elements with which said M was chosen from In (indium) and B (boron) AlaMbGa1-a-bN and here,

前記a及びbは、 $0<a\leqq 1$、
$0\leqq b<1$、
$a+b\leqq 1$

it is desirable to have the process which forms the numeric value to satisfy and the 2nd layer which comes out and consists of the ingredient shown one by one, and obtains a buffer layer, the process which forms the semiconductor region for semiconductor devices which consists of at least one nitride system compound semiconductor layer by vapor growth on said buffer layer, and the process which forms the 1st and 2nd main electrodes and control electrodes on the front face of said semiconductor region for semiconductor devices.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is rough **** central drawing of longitudinal section about following [HEMT] the 1st operation gestalt of this invention.
[Drawing 2] It is the top view of HEMT of drawing 1 .
[Drawing 3] It is the sectional view in which expanding the structure of HEMT of drawing 1 in order of a production process, and showing it.
[Drawing 4] It is the sectional view showing MESFET of the 2nd operation gestalt.
[Drawing 5] It is the sectional view showing the substrate of the 3rd operation gestalt, and a part of buffer layer.
[Drawing 6] It is the sectional view showing the substrate of the 4th operation gestalt, and a part of buffer layer.
[Description of Notations]
1 Substrate Which Consists of Silicon Single Crystal
2, 2a, 2b Buffer layer
8, 8a, 8b The 1st layer
9, 9a, 9b The 2nd layer
3 3a Semiconductor region

[Translation done.]

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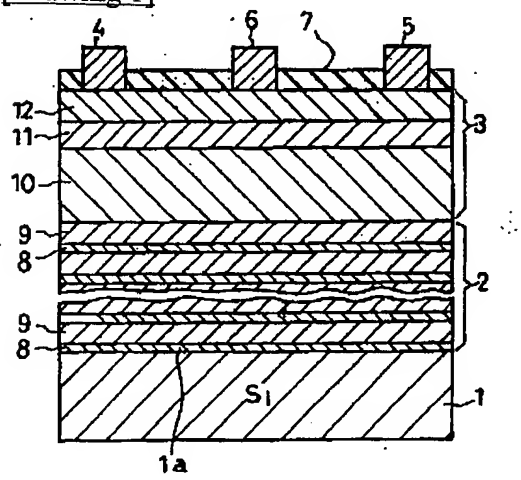
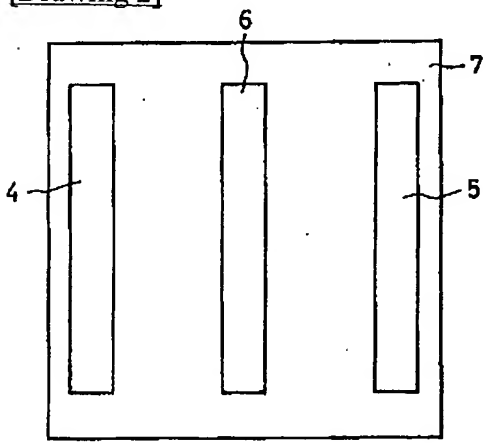
DRAWINGS

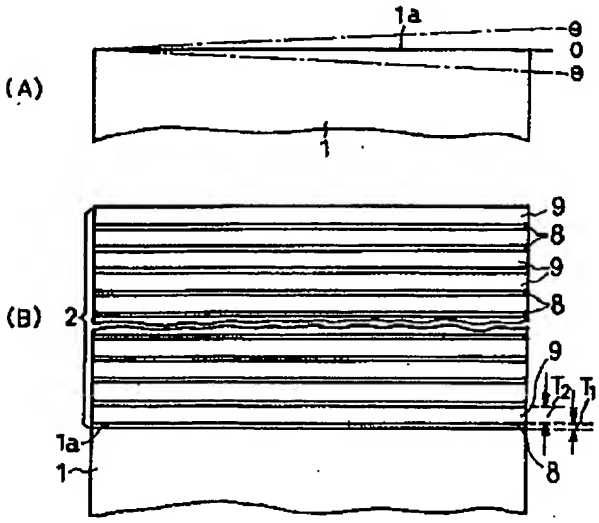
[Drawing 1]



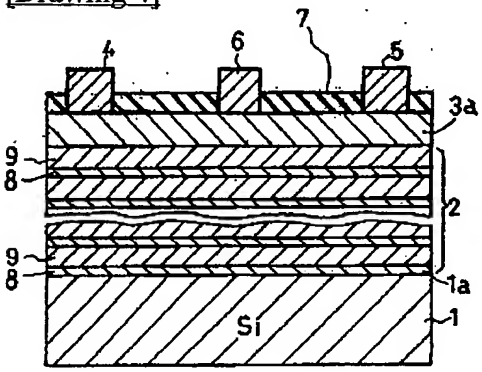
[Drawing 2]



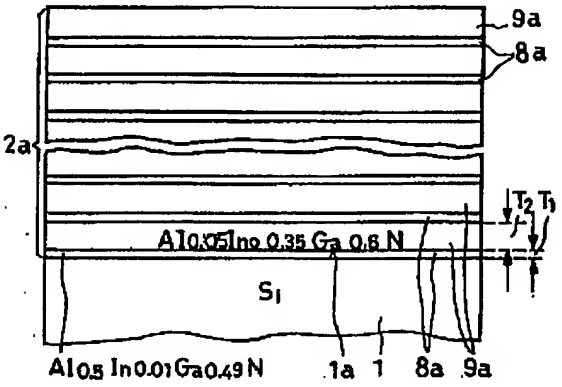
[Drawing 3]



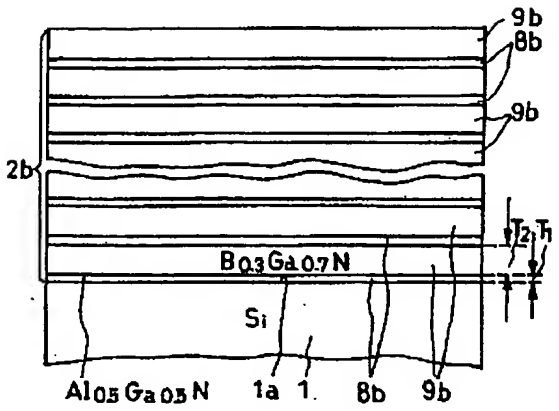
[Drawing 4]



[Drawing 5]



[Drawing 6]



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CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 2nd partition of the 7th section
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H01L 29/80 H
H01L 21/205
H01L 29/80 B
H01L 29/78 301 B

[Procedure revision]
[Filing Date] October 29, Heisei 16 (2004. 10.29)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] 0013
[Method of Amendment] Modification
[The contents of amendment]
[0013]
The HEMT element semiconductor region 3 has the electronic transit layer 10 which consists of impurity non-doping GaN, the spacer layer 11 which consists of non-doping aluminum0.2Ga0.8N, and the electronic supply layer 12 which consists of n form aluminum0.2Ga0.8N by which Si is doped as an n form impurity. Each class 10, 11, and 12 of the semiconductor region 3 for components consists of the gallium nitride system compound semiconductor which used nitrogen and a gallium as the base. The electronic transit layer 10 arranged on a buffer layer 2 can also be called a channel layer, and has the thickness of 500nm. It controls that the spacer layer 11 arranged on the electronic transit layer 10 has the thickness of 7nm, and the silicon as an n form impurity of the electronic supply layer 12 diffuses it in the electronic transit layer 10. The electronic supply layer 12 arranged on the spacer layer 11 can also be called a barrier layer, a layer of operation, or a channel layer, and has the thickness of 10nm. The source electrode 4 and the drain electrode 5 carry out ohmic contact at the electronic supply layer 12, and are carrying out Schottky contact of the gate electrode 6 to the electronic supply layer 12. In addition, the high contact layer of n form high impurity

concentration can be prepared between the source electrode 4 and the drain electrode 5, and the electronic supply layer 12. The insulator layer 7 which consists of SiO2 has covered the front face of a semiconductor region 3.
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] 0020
[Method of Amendment] Modification
[The contents of amendment]
[0020]
The desirable thickness of the 2nd layer 9 is 0.5nm - 200nm, i.e., 5-2000A. When the thickness of the 2nd layer 9 is less than 0.5nm, it becomes difficult to grow up evenly the semiconductor region 3 for components which grows on the 1st layer 8 and a buffer layer 2. Moreover, if the thickness of the 2nd layer 9 exceeds 200nm, with the compressive stress which originates in the stacking fault of the 2nd layer 9 and the 1st layer 8, and is generated in the 2nd layer 9, the electron density of the channel layer 10 will fall and the property of HEMT will deteriorate.
Furthermore, it is good preferably to make thickness of the 2nd layer 9 larger than the thickness of the 1st layer 8. If it does in this way, in holding down the distorted magnitude which originates in the stacking fault difference of the 1st layer 8 and the 2nd layer 9, and the coefficient-of-thermal-expansion difference of the 1st layer 8 and a substrate 1, and is generated in the 1st layer 8 to extent which a crack does not generate in the 1st layer 8, and maintaining at the concentration-of-electrons high concentration of the channel layer 10, it will become advantageous.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0031
[Method of Amendment] Modification
[The contents of amendment]
[0031]
[The 2nd operation gestalt]
Next, MESFET of the 2nd operation gestalt is explained with reference to drawing 4. However, in drawing 4, the same sign is substantially given to the same part with drawing 1, and the explanation is omitted.
MESFET of drawing 4 prepares n type semiconductor field 3a which consists the semiconductor region 3 of HEMT of drawing 1 of the GaN compound semiconductor layer by which Si was doped as an n form impurity, and forms others identically to drawing 1. That is, in MESFET of drawing 4, a silicon substrate 1, a buffer layer 2, the source electrode 4, the drain electrode 5, the gate electrode 6, and the insulator layer 7 are formed like what is shown with the same sign by drawing 1. N type semiconductor field 3a can also be called a channel layer or a barrier layer, and is arranged on the buffer layer 2. The source electrode 4 and the drain electrode 5 carry out ohmic contact at n type semiconductor field 3a, and are carrying out shot key barrier contact of the gate electrode 6 at n type semiconductor field 3a.
[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0035
[Method of Amendment] Modification
[The contents of amendment]
[0035]
2nd layer 9a
Chemical formula AlaInbGa1-a-bN
Here, a and b are 0<=a<1,
0<=b<1,
a+b<=1
The numeric value of the arbitration to satisfy,
It is the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9a was chosen from GaN, AlGaN, InGaN, and AlInGaN. For example, with the operation gestalt of drawing 5, aluminum0.05In0.35Ga0.6N equivalent to the ingredient with which a of said formula was set to 0.05, and b was set to 0.35 is used for 2nd layer 9a. It is smaller than the band gap of 1st layer 8a, the gap, i.e., the band gap, between the valence band of 2nd layer 9a and a conduction band.

[Procedure amendment 5]
[Document to be Amended] Specification
[Item(s) to be Amended] 0036
[Method of Amendment] Modification
[The contents of amendment]
[0036]
Next, 1st layer 8a explains the manufacture approach of buffer layer 2a that aluminum0.5In0.01Ga0.49N and 2nd layer 9a were set to aluminum0.05In0.35Ga0.6N.
Buffer layer 2a is formed on principal plane 1a of the same substrate 1 as the 1st operation gestalt. This buffer layer 2a is formed by repeating and carrying out the laminating of 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, and the 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N, well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, TMIn (trimethylindium) gas, and NH3 (ammonia) gas are supplied for about 24 seconds in a reaction chamber, and 1st layer 8a which changes from aluminum0.5In0.01Ga0.49N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 800 degrees C, the flow rate of 47micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas, i.e., the amount of supply of aluminum, / the flow rate of about 14micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 31micromol/min and TMIn gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas, TMG gas, and TMIn gas to 750 degrees C, TMA gas, TMG gas, TMIn gas, and NH3 (ammonia) gas are supplied for about 83 seconds after an appropriate time, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N whose thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8a. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 59micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TMA gas / the flow rate of 2.8micromol/min and TMG gas] into about 0.23 mol/min for the flow rate of 46micromol/min and TMIn gas. In this example, 1st layer 8a which repeats formation of 1st layer 8a which consists of above-mentioned aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N 10 times, and consists of aluminum0.5In0.01Ga0.49N, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N form buffer layer 2a by which the 20-layer laminating was carried out by turns. The 1st layer 8a which consists of aluminum0.5In0.01Ga0.49N, of course, and 2nd layer 9a which consists of aluminum0.05In0.35Ga0.6N are also changeable into the number of arbitration, such as 50 etc. layers, respectively.
[Procedure amendment 6]
[Document to be Amended] Specification
[Item(s) to be Amended] 0039
[Method of Amendment] Modification
[The contents of amendment]
[0039]
2nd layer 9b,
Chemical formula AlaBbGa1-a-bN
Here, a and b are 0<=a<1,
0<=b<1,
a+b<=1
The numeric value of the arbitration to satisfy,
It is the thin film of the semi-conductor which comes out and consists of the ingredient which can be shown. That is, 2nd layer 9b is a layer containing at least one element chosen from aluminum, B, and Ga, and N, for example, was chosen from GaN, BN, AlN, BGaN, AlGaN, AlBN, and AlBGaN, and is formed. With the operation gestalt of drawing 6, B0.3Ga0.7N equivalent to the ingredient with which a of said formula was set to 0 and b was set to 0.3 is used for 2nd layer 9b. It is smaller than the band gap of 1st layer 8b, the gap, i.e., the band gap, between the valence band of 2nd layer 9b, and a conduction band.
[Procedure amendment 7]

[Document to be Amended] Specification
[Item(s) to be Amended] 0040
[Method of Amendment] Modification
[The contents of amendment]
[0040]
Buffer layer 2b is formed by repeating and carrying out the laminating of 1st layer 8b which consists of aluminum0.5Ga0.5N, and the 2nd layer 9b which consists of B0.3Ga0.7N on principal plane 1a of a substrate 1 which has a field just (111), well-known MOCVD (Metal Organic Chemical Vapor Deposition), i.e., organic metal chemical-vapor-deposition method. That is, the substrate 1 of a silicon single crystal is arranged in the reaction chamber of an MOCVD system, first, thermal annealing is performed and a surface oxide film is removed. Next, TMA (trimethylaluminum) gas, TMG (trimethylgallium) gas, and NH3 (ammonia) gas are supplied for about 27 seconds in a reaction chamber, and 1st layer 8b which changes from aluminum0.5Ga0.5N whose thickness T1 is about 5nm, i.e., about 50A, to one principal plane of a substrate 1 is formed. In this example, after making whenever [stoving temperature / of a substrate 1] into 1080 degrees C, the flow rate of 31micromol/min and NH3 gas, i.e., the amount of supply of NH3, was set [the flow rate of TMA gas, i.e., the amount of supply of aluminum,] to about 0.14 mols / min for the flow rate of about 31micromol/min and TMG gas. Then, whenever [stop and stoving temperature / of a substrate 1] is lowered for supply of TMA gas to 1120 degrees C, TEB (triethyl boron) gas, TMG gas, and NH3 (ammonia) gas are supplied for about 85 seconds after an appropriate time, and 2nd layer 9b which consists of B0.3Ga0.7N of n form where thickness T2 is 30nm, i.e., 300A, is formed in the top face of 1st layer 8b. In addition, SiH4 gas can be supplied to coincidence and Si as an impurity can also be introduced into the formation film. In this example, the flow rate of 63micromol/min and NH3 gas, i.e., the amount of supply of NH3, was made [the flow rate of TEB gas, i.e., the amount of supply of boron,] into about 0.14 mol/min for the flow rate of 75micromol/min and TMG gas, i.e., the amount of supply of a gallium. In this example, 1st layer 8b which repeats formation of 2nd layer 9b which consists of the 1st layer 8b and B0.3Ga0.7N which consists of above-mentioned aluminum0.5Ga0.5N 50 times, and consists of aluminum0.5Ga0.5N, and 2nd layer 9b which consists of B0.3Ga0.7N form buffer layer 2b by which the 100-layer laminating was carried out by turns in total. 1st layer 8b which consists of aluminum0.5Ga0.5N, of course, and 2nd layer 9b which consists of B0.3Ga0.7N are also changeable into the number of arbitration, such as 25 etc. layers, respectively.
[Procedure amendment 8]
[Document to be Amended] Specification
[Item(s) to be Amended] 0042
[Method of Amendment] Modification
[The contents of amendment]
[0042]
[Modification(s)]
This invention is not limited to an above-mentioned operation gestalt, and the next deformation is possible for it.
(1) A substrate 11 can be used as silicon compounds, such as polycrystalline silicon other than single crystal silicon, or SiC.
(2) The electric conduction form of each class of semiconductor regions 3 and 3a can be made into an example and reverse.
(3) Each class of semiconductor regions 3 and 3a can be used as the gallium nitride system compound semiconductor or indium nitride system compound semiconductor chosen from GaN (gallium nitride), AlInN (indium nitride aluminum), AlGaN (gallium nitride aluminum), InGaN (gallium nitride indium), and AlInGaN (gallium nitride indium aluminum).
(4) In HEMT of drawing 1, the electronic supply layer 12 and the same electronic supply layer can be prepared between a barrier layer 10, i.e., an electronic transit layer, and a buffer layer 2.
(5) An insulated gate field effect transistor can be prepared instead of HEMT and MESFET.
(6) One layer can make [more] the number of buffer layers 2 and 2a and the 1st layers 8, 8a, and 8b of 2b than the 2nd layer 9, 9a, and 9b, and buffer layers 2 and 2a and the maximum upper layer of 2b can be used as the 1st layer 8, 8a, and 8b. Moreover, the one layer of the number of the 2nd layers 9, 9a, and 9b can also be conversely made [many] rather than the number of the 1st layers 8, 8a, and 8b.

(7) The 1st Layers 8, 8a, and 8b and 2nd layer 9, 9a, and 9b may contain an impurity in the range which does not check these functions.

[Translation done.]

NEW CENTRAL FAX NUMBER

Effective July 15, 2005

On July 15, 2005, the Central FAX Number will change to **571-273-8300**. This new Central FAX Number is the result of relocating the Central FAX server to the Office's Alexandria, Virginia campus.

Most facsimile-transmitted patent application related correspondence is required to be sent to the Central FAX Number. To give customers time to adjust to the new Central FAX Number, faxes sent to the old number (703-872-9306) will be routed to the new number until September 15, 2005. After September 15, 2005, the old number will no longer be in service and **571-273-8300** will be the only facsimile number recognized for "centralized delivery".

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